Unit- III
ANALOG ELECTRONICS

INTRODUCTION:

Electronic Components:

* Electronic components are classified into active and passive components.
* Active components supply energy to the circuit. Eg: Battery, semiconductor devices etc.
* Passive components consume energy from the source.
  Eg: Resistors, Capacitors, Inductors etc.

RESISTORS (R)

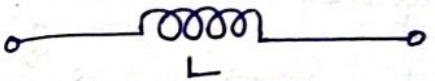
* R is an electrical / electronic component used to limit the flow of current.
* Unit is ohm (Ω)
* Symbol:

* $R = \frac{V}{I}$ (By Ohm's law)
* $R = \frac{\rho l}{A}$

$R \rightarrow$ Resistance in ohm
$\rho \rightarrow$ Resistivity of the wire in ohm-cm
$l \rightarrow$ Length of the wire in cm.

INDUCTOR (L):

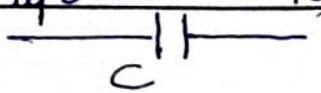
It is used to store the energy in the form of magnetic energy, when electricity is applied to it. The SI unit of inductor is Henry (H).



$L = \frac{\phi(i)}{i}$; $L \rightarrow$ Inductance
$\phi(i) \rightarrow$ Magnetic flux of current i
$i \rightarrow$ Current.

CAPACITOR

Capacitor is used to store the energy in the form of electrical charge producing a potential difference across the plates.
S.I unit of capacitor is Farad (F).



$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$

C → Capacitance of a Capacitor
ε_0 → Permittivity of free space
ε_r → " " dielectric medium
d → Distance between plates.
A → Area of two conducting plates

$$C = \frac{Q}{V}$$

Q → Charge
A → Area

SEMICONDUCTOR MATERIALS

Semiconductor is a material that has conductivity level between extremes of insulator and conductor.

Semiconductor
- Intrinsic Semiconductor (Pure form)
- Extrinsic Semiconductor
  - n-type
  - p-type.

The process of adding impurity to a pure semiconductor is called doping.

Types: n-type, P-type.

N-type Semiconductor:

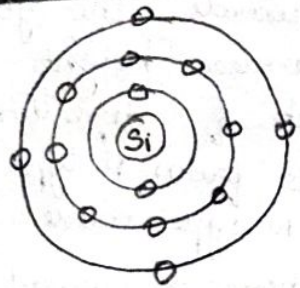
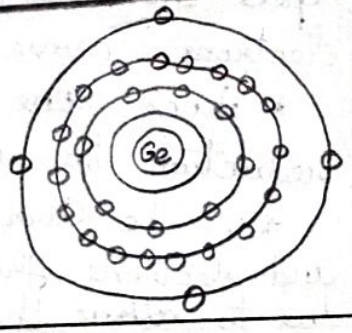
This is formed by doping pentavalent impurity atoms like arsenic, antimony or phosphorus. This process creates excess unbond electrons.

P-type Semiconductor:

This is formed by doping trivalent impurity like Aluminium or boron. This process creates excess holes.

Silicon and Germanium:

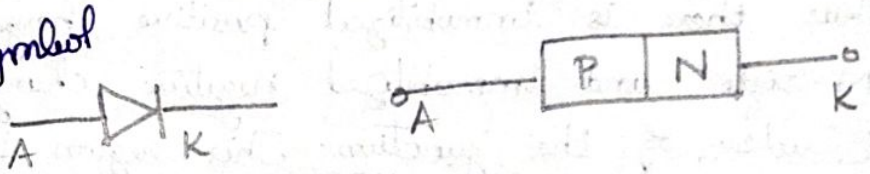
* Silicon and Germanium, are both in the same group (group 14) of the periodic table.
* Both have 4 valence electrons in the outer shell.
* Both have similar physical and chemical characteristics.
* Both are metalloids.

Parameter	Silicon	Germanium
Definition	Silicon is chemical element with atomic number 14 & symbol Si	Germanium is a chemical element with atomic number 32 & symbol is Ge.
Electron Configuration	1S2 2S2 2P6 3S2 3P2	1S2 2S2 2P6 3S2 3P6 4S2 3d10 4P2
D electrons	Has no d electrons	Has d electrons
Atomic Radius	Has a smaller atomic radius than Germanium	Has comparitively a larger atomic radius
Conductivity	Comparatively low	Conductivity is comparatively higher.
Semiconductor	Widely used because they are used at higher temperatures.	Widely not used because of temperature limits
Atomic Structure		

PN Junction Diode:

A PN junction diode is formed when n-type and p-type semiconductors are joined together.

Symbol

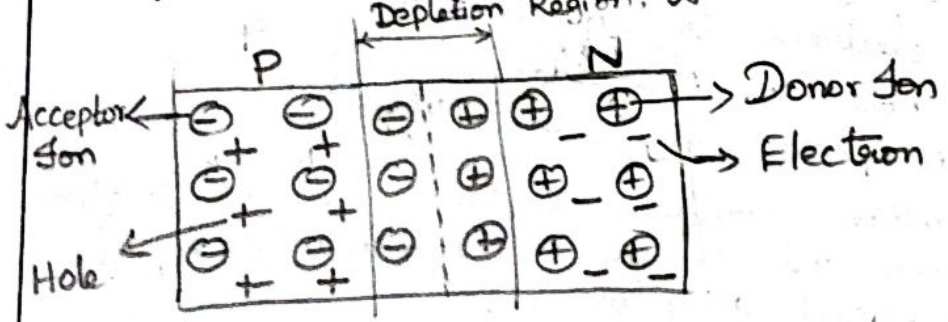


In N-type material,
Majority Carriers – electrons
Minority Carriers – holes

In P-type material,
Majority carriers – holes
Minority carriers – electrons

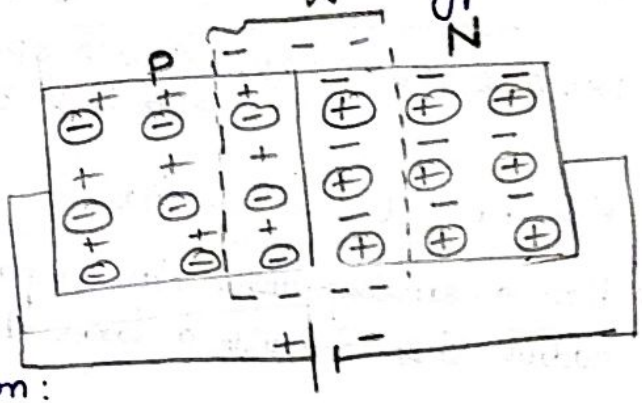
* At the junction there is a tendency for free electrons to diffuse over the P-side and hole to N-side.
* This process is called diffusion.
* Electrons combine with holes in P-type material and creates a negatively charged immobilized acceptor ions.

* Similarly the holes move into N-material and combine with free electrons of the donor atoms and creates immobilized donor ions.
* Thus there is immobilized positive charge on N-side and immobilized negative charge on P-side of the junction. This region is known as Depletion region (or space charge region or transition region).
* It creates a built-in potential or barrier potential, V_b across the junction.
* The barrier potential V_b is
  0.3 V for Germanium.
  & 0.7 V for Silicon.



Diode under Forward Bias Condition:

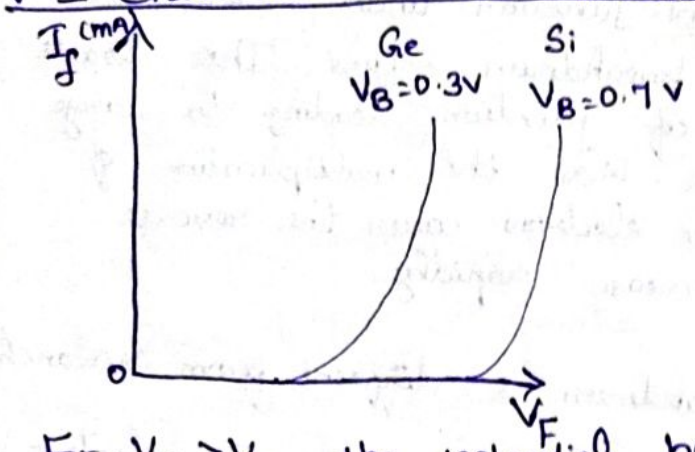
This is done by connecting positive terminal of battery to P-type and its negative terminal to N-type as in figure.



Operation:

* Under Forward bias, the applied positive voltage repels the holes in P-type and holes move towards the junction.
* Similarly, the applied negative voltage repels the electrons in N-type region and electrons move towards the junction.
* Hence the barrier height reduces with reduction in width of depletion region.
* ∴ The holes from P-type move to N-type and electrons from N-type move towards P-type and due to this there is current flow & it is called as forward current, I_f.

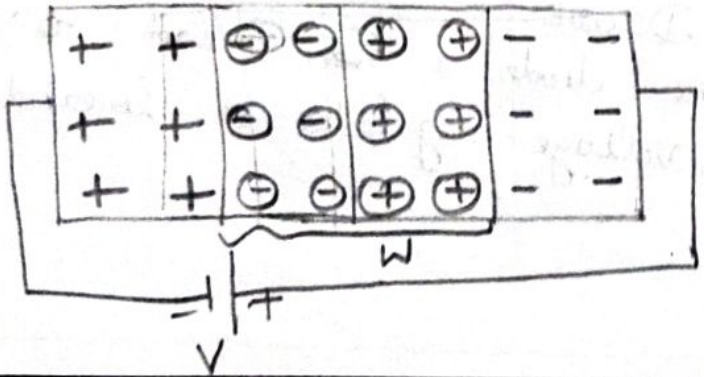
V-I Characteristics under Forward Bias:



For $V_F > V_B$, the potential barrier disappears at the junction and large current, I_f flows.

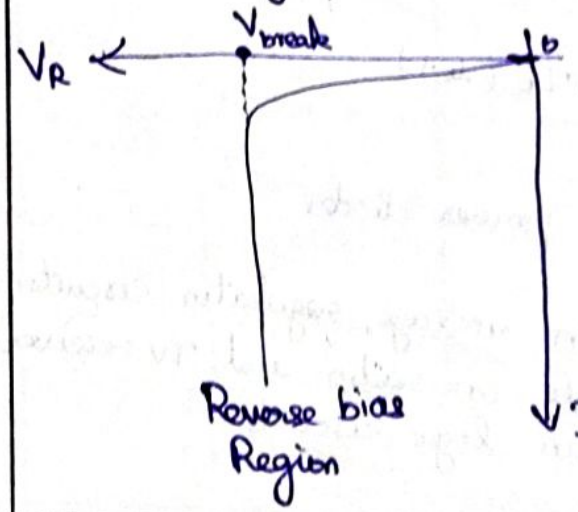
Diode under Reverse Bias Condition:

Reverse bias is obtained by connecting positive terminal of the battery to N-type and negative terminal to the P-type.



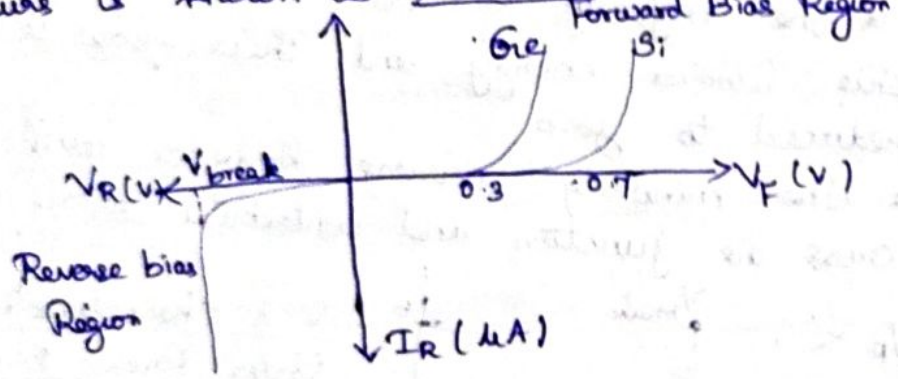
Operation:

* Under Reverse bias, the majority electrons are attracted by positive terminal and majority holes are attracted by negative terminal of battery.
* As a result, the depletion region is widened and the barrier potential rises.
* The majority carriers cannot overcome this barrier energy and their flow is reduced to zero.
* The minority carriers however will cross the junction and contributes reverse current I_R.



V-I Characteristics Under Reverse Bias

For large applied reverse bias voltage, electrons move towards positive terminal of battery. Since a large number of electrons are formed, it is called avalanche of free electrons. This leads to breakdown of junction leading to large reverse current. The reverse voltage at which the junction breakdown occurs is known as breakdown voltage.



Diode Applications:

1) As rectifiers or power diodes
2) As signal diodes
3) As Zener diode in voltage regulator circuits.
4) As Varactor diode in radio and TV receiver
5) As a switch in logic circuits.

Avalanche Effect:

In PN-junction under reverse bias the avalanche breakdown occurs. This leads to breakdown of junction leading to large reverse current. Here the multiplication of number of free electrons causes the reverse current to increase rapidly.

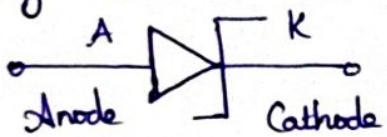
Zener Effect:

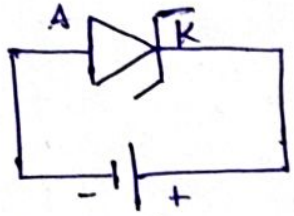
* Zener breakdown is different from avalanche breakdown.
* Zener breakdown occurs when the electric field in the depletion layer increases and it breaks covalent bond and generates electron-hole pair
* In this a large number of carries are generated.
* This process is quantum tunneling.

ZENER DIODE:

A Zener diode is also called as voltage refference, voltage regulator or breakdown diode.

Symbol

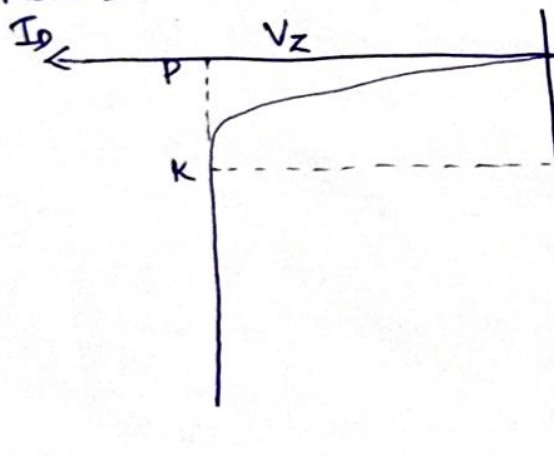




Circuit diagram

* Zener diode is operated in the reverse bias breakdown region.
* The breakdown voltage of a Zener diode is set by controlling the doping level during manufacture.

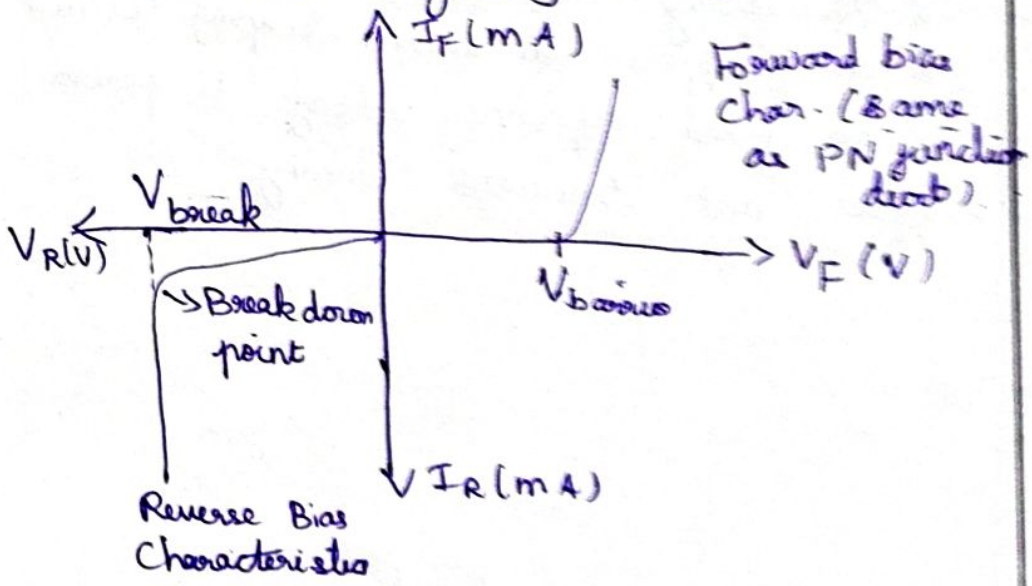
Reverse Characteristic of Zener Diode:



* Zener diode is operated in reverse bias only.

Fig: Reverse Characteristic of a Zener Diode.

* Zener diode is operated only in the reverse-bias region.
* From fig. the reverse voltage (V_R) is increased, the reverse current (I_Z) remains negligibly small upto the 'knee' of the curve point 'P'.
* At this point, the effect of breakdown process begins.
* From the bottom of knee, the breakdown voltage, V_Z remains constant. This ability of a diode is called regulating ability.



* There is a minimum value of Zener current called breakover current ($I_{Z\,min}$) which must be maintained in order to keep the diode in breakdown or regulation region.
* When the current is reduced below knee, the voltage changes drastically and regulation is lost.
* Above the maximum value of Zener current $I_{Z(max)}$ the diode may be damaged.

Applications :

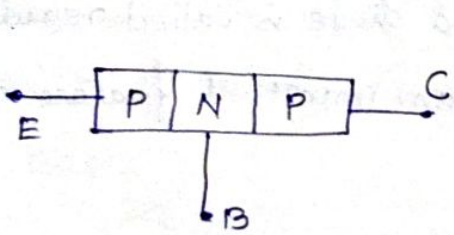
* As Voltage Regulator
* As Clippers in wave-shaping circuits
* As fixed reference voltage is power supplies and transistor biasing.

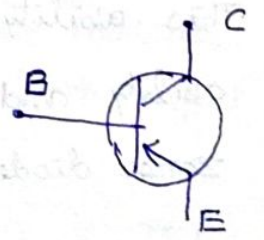
TRANSISTOR

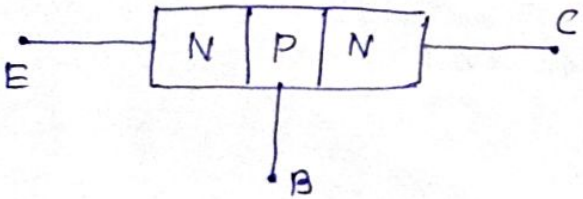
* A bipolar junction transistor is a three-layer two junction and three-terminal Semiconductor device.
* It's operation depends on the interaction of majority and minority carriers. Therefore it is named as bipolar device.

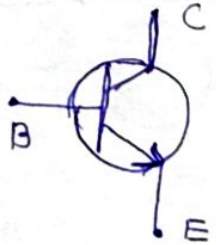
(TRANSfer + RESISTOR ⇒ Transistor)

* Transistor means, signals are transferred from low resistance circuit (input) into high resistance (output) circuit.









Emitter:-

It is more heavily doped than any of other regions because its main function is to supply majority charge carriers to the base.

* The current through the emitter is emitter current. It is denoted as I_E.

Base:-

* Base is the middle section of the transistor.
* It separates the Emitter and Collector.
* It is very lightly doped. It is very thin as compared to either Emitter (or) collector.
* The current flows through the base section is base current, and its denoted as "I_B".

Collector:-

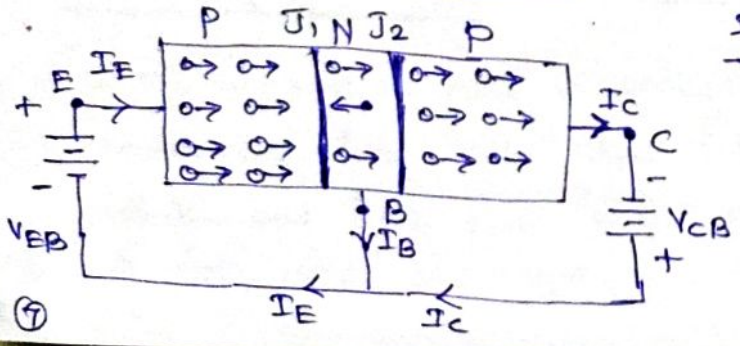
* The main function of the collector is to collect the majority charge carriers coming from the Emitter and passing through the Base.
* It is a moderately doped. The current flows through Collector is Collector Current. It is denoted as I_C.

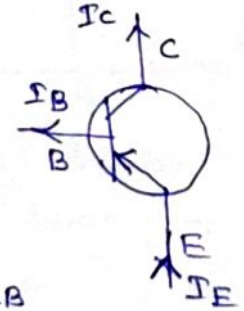
Types:-

PNP & NPN Transistors.

* Emitter section is always to provide charge Carriers, therefore, it is always forward biased.
* First letter of transistor type indicates the polarity of the emitter voltage with respect to base.
* The main function of Collector is to Collect (or) attract those Carriers through the base, hence it is always reverse biased.
* Second letter of transistor type indicates the polarity of Collector voltage with respect to the Base.

Working of PNP -Transistor

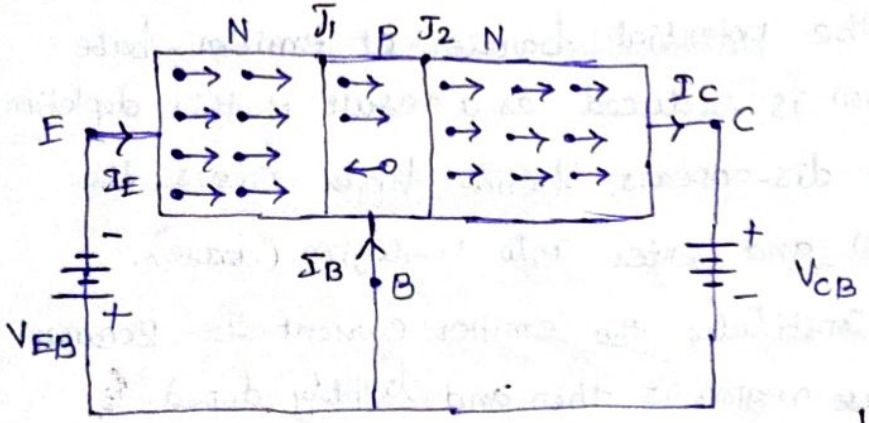


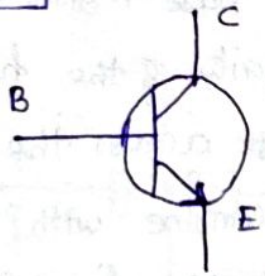


* The above diagram shows the Connection of PNP-Transistor.
* Here, the emitter - base junction is forward biased, and Collector - base junction is reverse biased.
* The holes in the emitter are repelled by the positive terminal of battery.
* Then the potential barrier at emitter - base junction is reduced as a result of this depletion region dis-appears, hence holes cross the junction and enter into N-region (base).
* This Constitutes the emitter current I_E. Because the base region is thin and lightly doped. majority of the holes (about 97.5%) are able to drift across the base without meeting electrons to combine with only 2.5% of the holes recombine with the free electrons (or) N-region.
* This constitutes the base current I_B, which is very small.
* The holes which after crossing the N-P Collector Junction enter the Collector region.

* They are swept out by the negative Collector voltage V_{CB}. This constitutes the Collector current I_C. $I_C = I_E - I_B$, $I_E = I_B + I_C$

Working of N-P-N Transistor





* In this Circuit diagram, the Emitter - Base junction is forward biased. (i/e negative polarity of the battery (V_{EB}) is connected to N-type Emitter terminal.
* Similarly, the Collector - Base junction (J_2) is reverse biased by connecting +ve terminal of battery with Negative (N-type) material.
* The electrons in the emitter region are repelled by the negative battery terminal towards the emitter junction.
* The electron crossover into the p-type base region because potential barrier is reduced due to forward bias, and base region is very thin and highly doped.
* Most of the electrons (about 97.5%) cross-over to the Collector junction and enter the Collector region, where they are readily swept up by the positive Collector voltage V_{CB}. Only 2.5% of the emitter electrons combine with the holes in the base and are lost as charge Carriers.

TRANSISTOR- CONFIGURATIONS

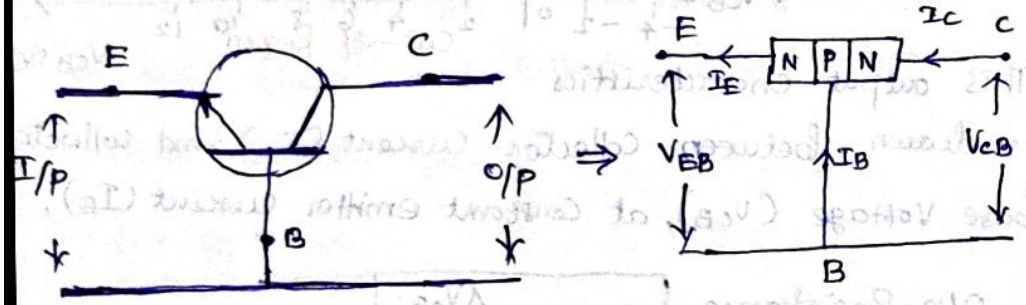
There are 3-Configurations.

1. Common-Base Configuration
2. Common-Emitter Configuration
3. Common-Collector Configuration.

COMMON-BASE CONFIGURATION

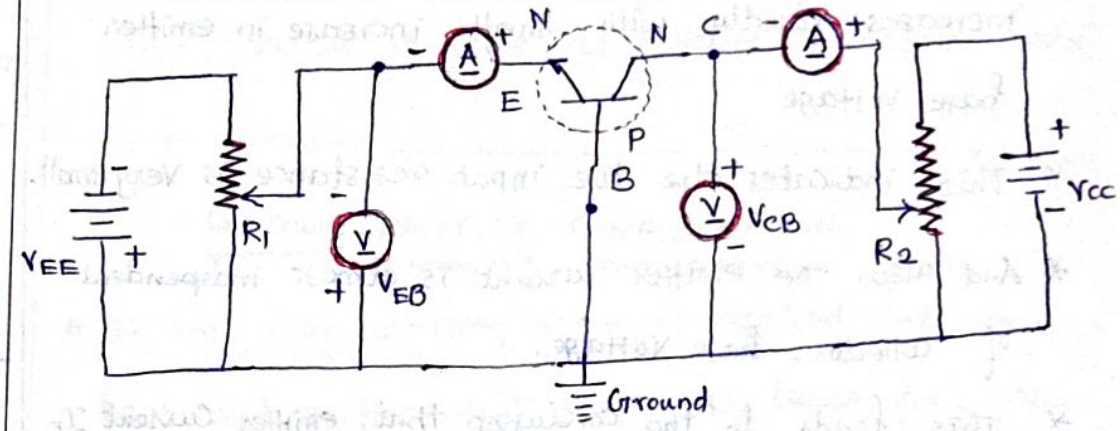
* In this Configuration, base terminal acts as a Common-terminal for input and output.

Diagram:-



* In this configuration, input is applied between emitter and base while output is taken from collector and base. Here, Base acts as a common to both input and output.

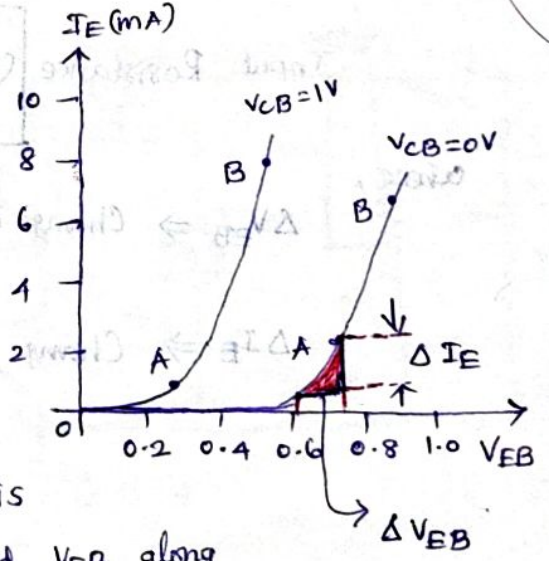
Input and output Characteristics:-



* This diagram, shows, how the input (I_E) emitter current varies with input voltage V_{EB}, when output voltage V_{CB} is held constant.

* To determine the input Characteristics initially, the output voltage V_{CB} is set as zero, then the input voltage V_{EB} is increased.

* The input charateristics drawn between emitter current I_E and emitter-base voltage V_{EB}.



* The emitter current (I_E) is taken along y-axis and V_{EB} along x-axis.

* From the above graph, the emitter current (I_E) increases rapidly with small increase in emitter base voltage.
* This indicates the the input resistance is very small.
* And also, the emitter current is almost independent of collector - base voltage.
* This leads to the conclusion that, emitter current I_E and hence collector current (I_C) is almost independent of collector - base voltage (V_{CB}).
* This input characteristics used to find the input resistance of the transistor.

Input Resistance $(R_{in}) = \dfrac{\Delta V_{EB}}{\Delta I_E}$ at constant V_{CB}

where,

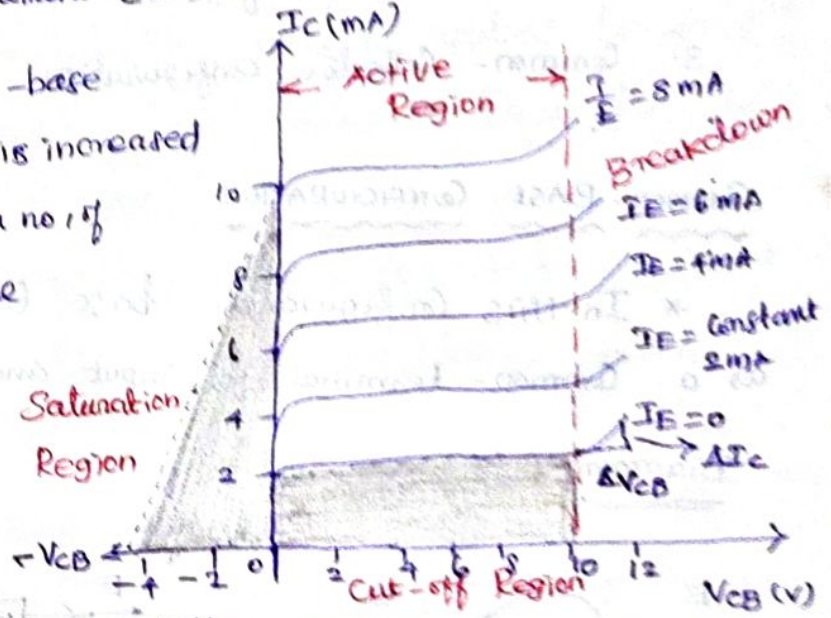
ΔV_{EB} ⇒ Change in Emitter - Base junction voltage

ΔI_E ⇒ Change in Emitter - Current.

Output Characteristics:-

To determine the output characteristics, the emitter current I_E is kept constant, at a suitable value by adjusting the emitter-base voltage V_{EB} and varying R_2 and output current (I_C) is measured.

* The collector-base voltage (V_{CB}) is increased from zero in a no. of steps, and the corresponding collector current (I_C) is noted.



* This output characteristics is drawn between collector current (I_C) and collector-base voltage (V_{CB}), at constant emitter current (I_E).
* O/p Resistance $R_{out} = \dfrac{\Delta V_{CB}}{\Delta I_C}$
* This Characteristic is used to find amplification factor $\alpha = \dfrac{\Delta I_C}{\Delta I_E}$

Saturation Region:-

* It is the region left to the vertical line. In this region, Collector - base voltage V_{CB} is negative. i.e the collector base junction is also forward biased and a small change in V_{CB} results in larger variation in Collector Current.

Active Region:-

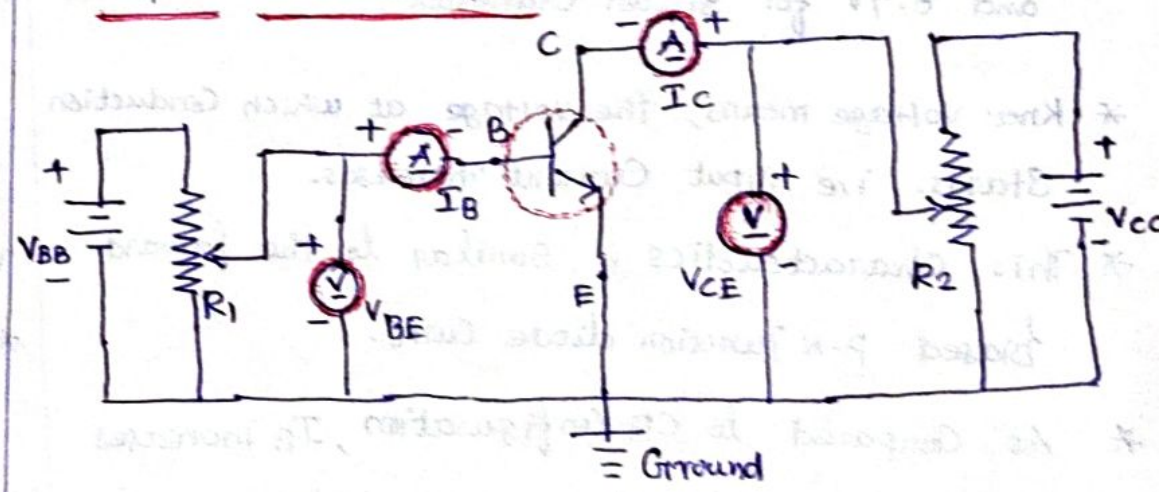
* It is the region, between the vertical line to horizontal axis.
* In this region, the Collector Current is almost Constant and is equal to the emitter Current.
* In this region, the emitter base junction is forward biased and Collector - base junction is reverse biased.

Cut-off Region:-

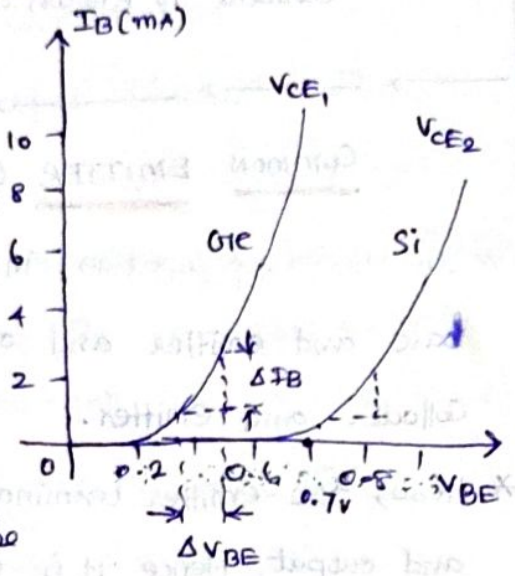
* It is the region along the horizontal axis.
* In this region, both junctions are reverse biased.
* Due to this, there is no current flow in Collector terminal due to majority Carriers.
* But due to minority Carriers, current will flow. This Current is known as reverse saturation Current.

COMMON EMITTER CONFIGURATION

* In this Configuration, input is applied between base and emitter and output is taken from the Collector and emitter.
* Here, the emitter terminal is Common to both input and output. Hence it is called Common-Emitter Configuration.
* Input Characteristics:-



* The above diagram shows the circuit diagram for Common-emitter configuration.



* At constant V_{CE}, the input current I_B varies with the variation of V_{BE}.

* If the input voltage (V_{BE}) is less than threshold (or) knee voltage below which the base current is very small.

* The value of knee voltage is 0.3V for germanium and 0.7V for silicon transistor.

* Knee voltage means, the voltage at which conduction starts. i.e input current increases.

* This characteristics is similar to the forward biased P-N junction diode curve.

* As compared to CB configuration, I_B increases less rapidly with V_{BE}.

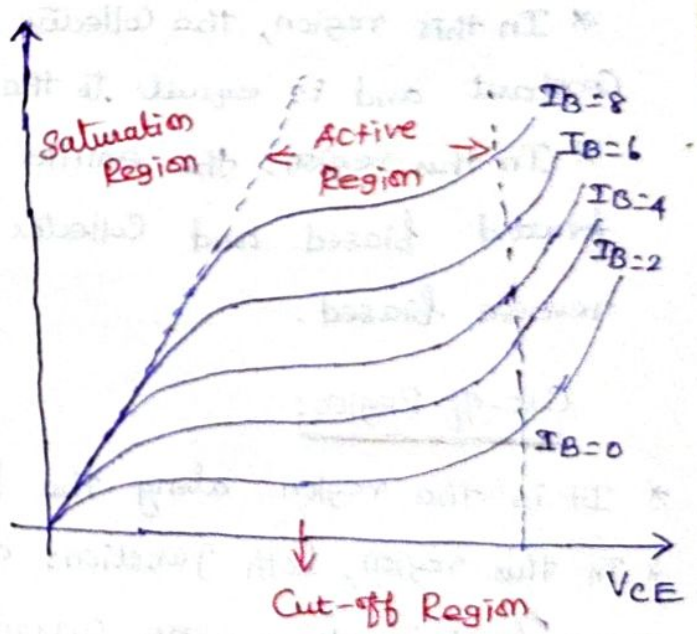
* Therefore, input resistance of a CE configuration is higher than that of CB configuration.

* Input resistance

$$R_{in} = \frac{\Delta V_{BE}}{\Delta I_B}$$ at constant V_{CE}

Output Characteristics :-

It is a curve between collector current and collector-emitter voltage at constant base current (I_B)



* From the graph, V_{CE} increases from zero to one volt, collector current I_C rapidly increases.

* This region is called saturation region.

We know that $\frac{1}{1-\alpha} = \beta + 1 = \gamma$

Therefore $I_E = I_B(\beta + 1) + I_{CBO}(\beta + 1)$

3.15 COMPARISON OF CB, CE AND CC CONFIGURATION

No.	Property	CB	CE	CC
1.	Input resistance	Low ($R_{in} = \frac{\Delta V_{EB}}{\Delta I_E}$) (about 100Ω)	Moderate ($R_{in} = \frac{\Delta V_{BE}}{\Delta I_B}$) (about 750Ω)	High ($R_{in} = \frac{\Delta V_{BC}}{\Delta I_B}$) (about 750)
2.	Output resistance	High ($R_{out} = \frac{\Delta V_{CB}}{\Delta I_C}$) (about 450Ω)	Moderate ($R_{out} = \frac{\Delta V_{CE}}{\Delta I_C}$) (about 45Ω)	Low ($R_{out} = \frac{\Delta V_{CE}}{\Delta I_E}$) (about 25Ω)
3.	Current gain	1	High (100)	High (100)
4.	Voltage gain	About 150	About 150	Less than unity
5.	Phase shift between input and output voltage	0 (or) 360^0	180^0	0 or 360^0
6.	Leakage current	Very small	Very large	Very large
7.	Applications	Used in high frequency applications	Used in audio frequency applications	For impedance matching
	Current Amplification Factor	$\alpha = \frac{\Delta I_C}{\Delta I_E}$	$\beta = \frac{\Delta I_C}{\Delta I_B}$	$\gamma = \frac{\Delta I_E}{\Delta I_B}$

Current Amplification Factor

In a transistor amplifier with AC input signal, the ratio of change in output current to the change in input current is known as *current amplification factor.*

In CB configuration,

The current amplification factor $\alpha = \frac{\Delta I_C}{\Delta I_E}$ ... (1)

In CE configuration,

The current amplification factor $\beta = \frac{\Delta I_C}{\Delta I_B}$ ... (2)

* After this, Collector Current I_C becomes almost constant, and independent with V_{CE}.

* This value of V_{CE} upto which Collector Current I_C changes is called the "knee Voltage".

* when $I_B = 0$, a small amount of Collector Current flows. It is called reverse saturation Current (I_{CEO}). Since the main Collector Current is zero, the transistor is said to be cut-off region.

* It may be noted that, if V_{CE} is increased continuously, then deption region in CB junction increased, it increases I_C and operates the transistor in active region.

* Further increase in V_{CE} causes avalanche breakdown in CB junction as a result of this, enormous I_C will flow and the transistor enters into breakdown region.

* This characteristics can be used to find Current gain β. It is defined as the ratio of change in output current (ΔI_C) to the change in input Current (ΔI_B).

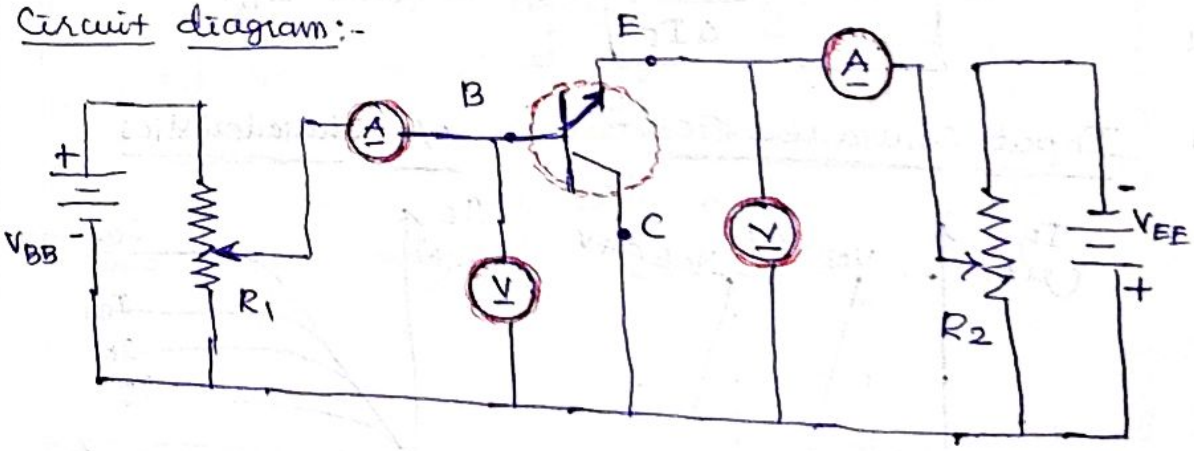
$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

* Output resistance $R_{out} = \frac{\Delta V_{CE}}{\Delta I_C}$ at Constant I_B.

COMMON COLLECTOR CONFIGURATION

In this configuration, Collector terminal is common to input and output.

Circuit diagram:-



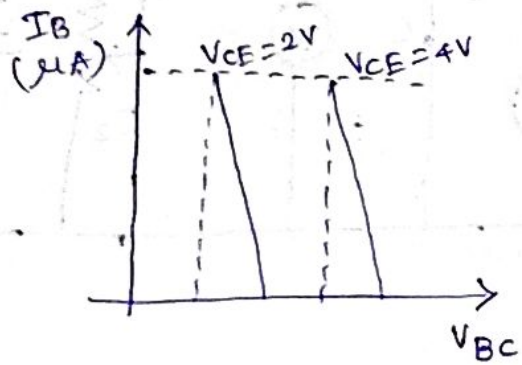
* The above diagram shows the Circuit diagram of Common Collector Configuration.

* To determine the output characteristics, the base current I_B is kept constant. At a suitable value by adjusting the base-Collector voltage and varying R_2 and the output current (Emitter current I_E) is measured.

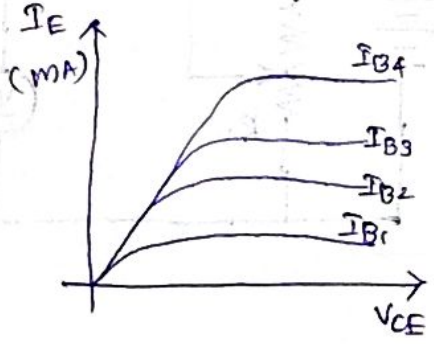
* Since I_C is approxi-mately equal to I_E, thus Common Collector Characteristics is identical to CE-configuration.

$$R_{out} = \frac{\Delta V_{CE}}{\Delta I_E}$$ at Constant I_B.

Input characteristics:-



o/p Characteristics



* This characteristics may be used to find current amplification factor(ν).

$$\nu = \frac{\Delta I_E}{\Delta I_B}$$ at Constant V_{CE}

FIELD EFFECT TRANSISTOR:

* FET is a device in which the flow of current through the conducting region is controlled by electric field.
* Hence the name is called as Field Effect Transistor (FET).
* Current conduction is only by majority carriers. ∴ FET is said to be unipolar device.
* Based on construction, FET is classified into two types.

i) Junction Field Effect Transistor (JFET)

ii) Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

i) JFET

JFET is classified into two types.

Depending on the majority carriers,

i) N-Channel JFET

ii) P-Channel JFET

N-Channel JFET
- majority carriers are electrons.

P-Channel JFET
- majority carriers are holes.

N-Channel JFET:

It consists of N-type silicon base. The small piece of P-type materials is are attached to its sides forming P-N junction.

Source (S): Through which the majority carriers enters into N-Channel bar.

Drain (D): Through which the majority carriers leaving from N-channel bar.

Gate (G): Heavily doped P-type silicon is diffused on both sides of N-type bar. Both junctions are connected to form gate.

Channel: The region between two depletion region is said to be n-channel.

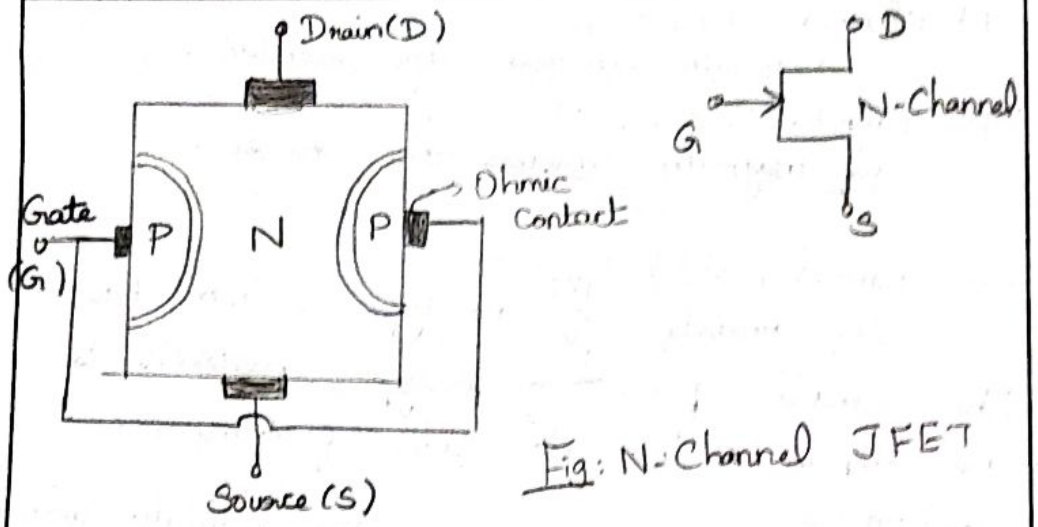


Fig: N-Channel JFET

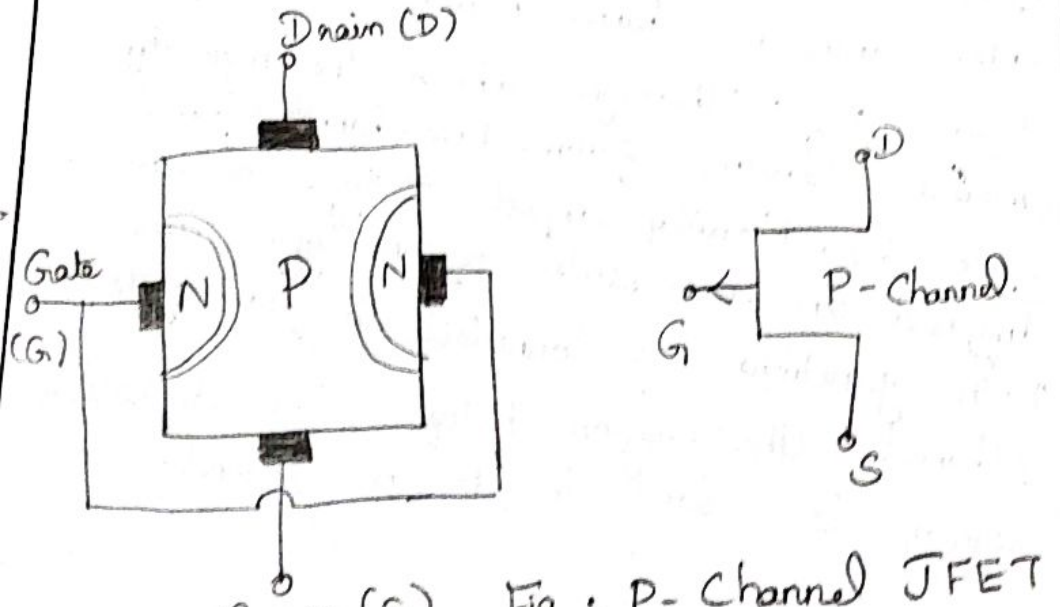


Fig: P-Channel JFET

It consists of N-type N-type silicon bars. The small pieces of P-type material are attached to its sides forming PN-junction.

Source (S): Through which the majority carriers enters into N-channel bar.

Drain (D): Through which the majority carriers leaving from the N-channel bar.

Gate (G): Heavily doped P-type silicon is diffused on both side of N-type bar. Both junctions are connected to form gate.

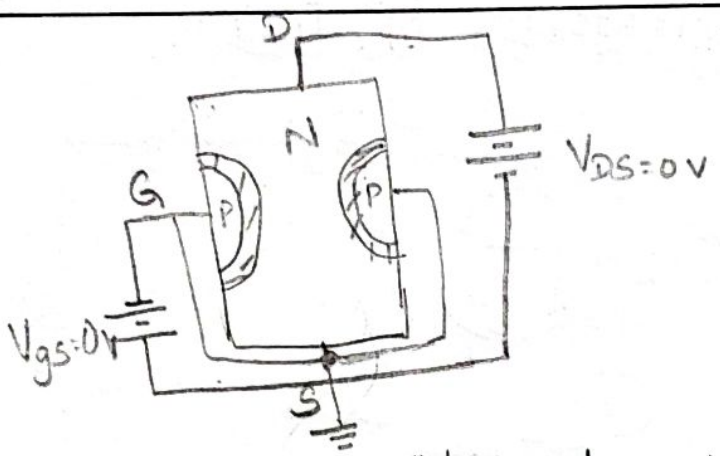
Channel:

The region between two depletion region is said to be N-channel.

Operation:

(1) When $V_{GS} = 0$ & $V_{DS} = 0$

When no voltage is applied between drain and source, and gate to source the thickness of depletion region is uniform; as shown in diagram.

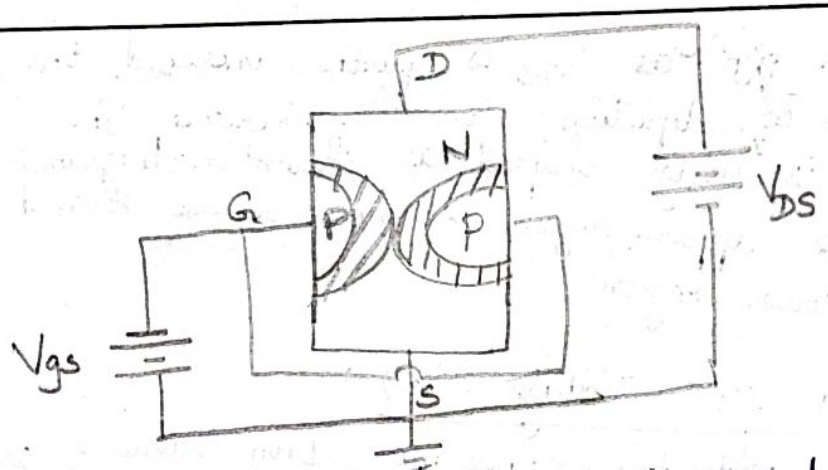


ii) When $V_{DS} = 0V$ & V_{GS} is decreased from Zero:

In this case, PN junctions are reverse biased. Hence thickness of the depletion region is increased. As V_{GS} is further decreased from zero, the reverse biased voltage is increased. Hence thickness of the depletion regions are also increased until the 2 depletion regions contact with each other. This condition in said to be cut-off.

Cut-off Voltage [$V_{GS(OFF)}$]:

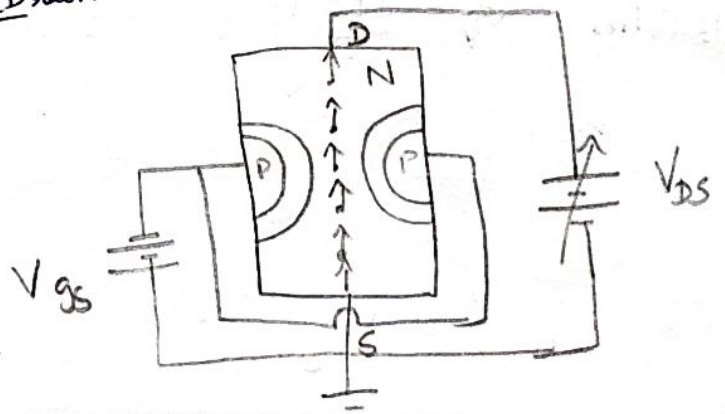
The V_{GS} value at which the I_D current ~~sett~~ cut-off in JFET is called cut-off voltage (or) $V_{GS(OFF)}$



(iii) When $V_{GS} = 0$ and V_{DS} is increased from 0

As shown in diagram drain is positive with respect to source with $V_{GS} = 0V$.

Now the majority carriers (electrons) flow through the N-channel from source to drain. I_D (Drain current) flow from drain to source.



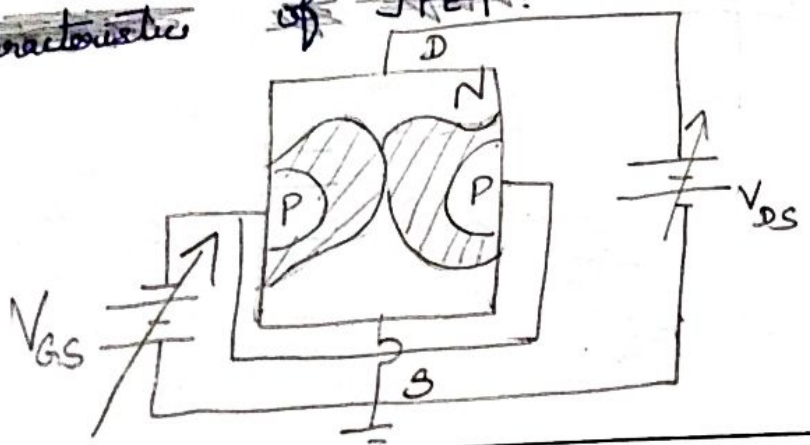
From fig. as V_{DS} is further increased, the thickness of depletion region also increases. The Channel is wedge shaped as shown in diagram. Hence, upper region is more reverse biased than lower region.

PINCH- OFF Voltage (V_p):

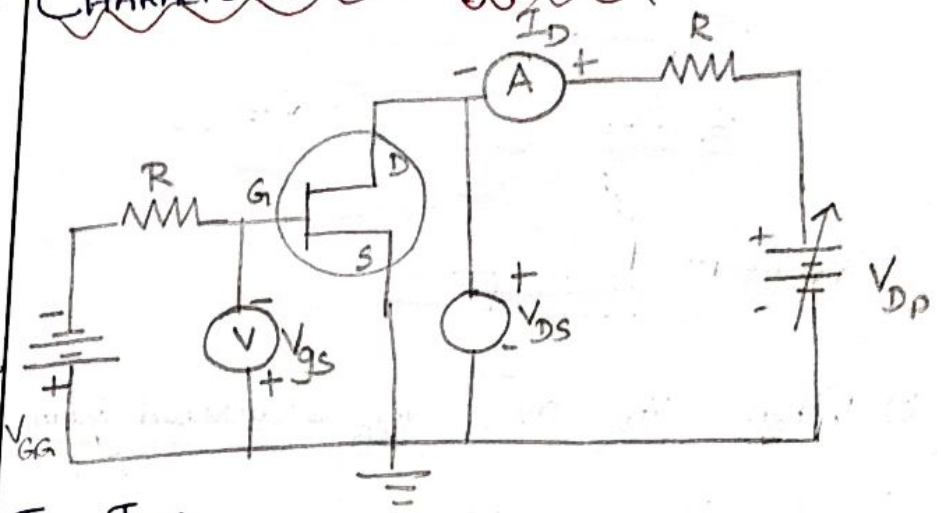
At the ~~constant~~ certain value of V_{DS}, the cross sectional area (Channel path) of JFET becomes minimum.

At this voltage the channel is said to be pinch off and the voltage (V_p) is so called pinch off voltage.

Characteristics of JFET:



CHARACTERISTICS OF JFET:

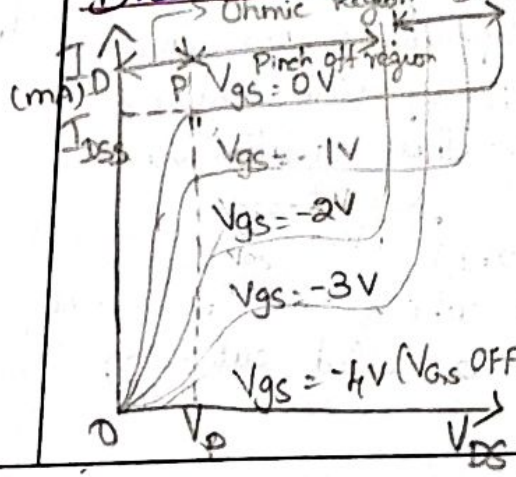


Two Types

(i) Drain Characteristics

(ii) Transfer Characteristics

Drain Characteristics:



As in graph, V_{DS} is increased from zero, I_D increases along V_p. and the rate of increase of I_D with V_{DS} decreases. The region from $V_{DS} = 0V$ to $V_{DS} = V_P$ is called ohmic region.

ΔI_E

In Ohmic region, the drain to source resistance $\frac{\Delta V_{DS}}{\Delta I_D}$ is related to gate voltage V_{GS}

When $V_{DS} = V_P$, I_D becomes maximum. When V_{DS} is increased beyond V_P, the length of the pinch-off (or) saturation region increases

Hence, there is no further increase of I_D. At a certain voltage corresponding to the point 'B', I_D suddenly increases.

This effect is due to the Avalanche multiplication of electrons caused by breaking of covalent bonds.

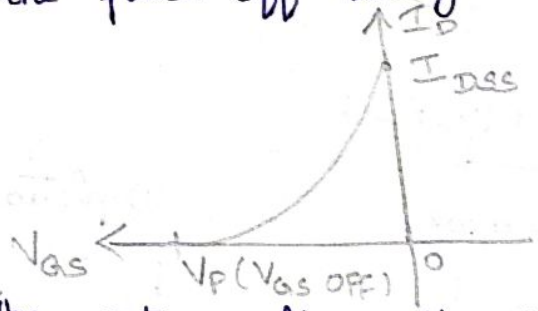
The drain voltage (V_{DS}) at which the breakdown occurs is denoted by BV_{DSO}

When $V_{GS} = 0V$, variation of I_D with V_{DS} is shown as curve OABC.

When V_{GS} is negative & V_{DS} is increased when gate is maintained at negative voltage ($V_{GS} = -1V$, $V_{GS} = -2V$, ...) The reverse voltage across the junction is further increased. Hence, I_D current decreases than above the pinch off voltage

Transfer Characteristics

For the transfer characteristics V_{DS} is kept constant at a suitable value greater than the pinch off voltage (V_P).



The gate voltage V_{GS} is decreased from zero till I_D is reduced to zero. The transfer characteristics I_D Vs V_{GS} is shown in graph.

Applications of JFET:

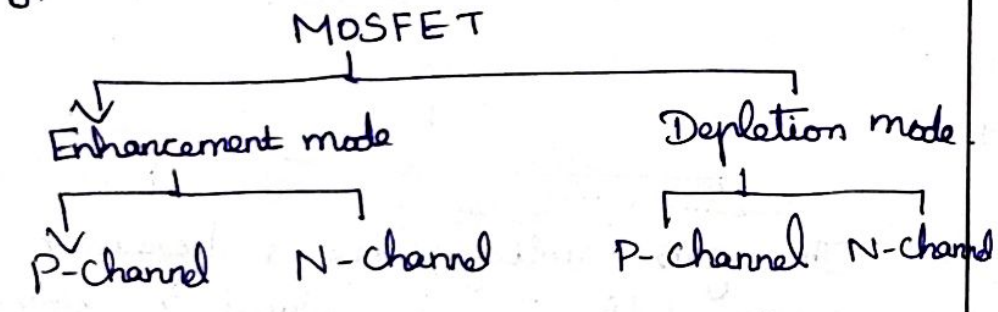
1) Used as an electronic switch.
2) Used as an amplifier
3) Used as chopper.
4) Used as buffer
5) Used in digital circuits.

CHENNAI INSTITUTE OF TECHNOLOGY SCIENCE AND HUMANITIES

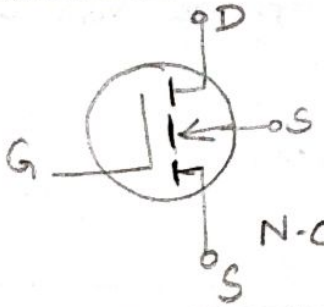
METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

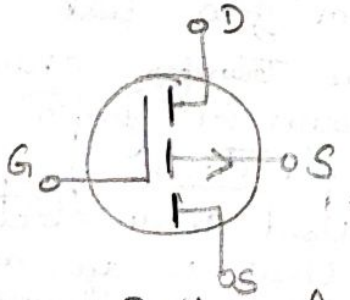
* MOSFETs are electronic devices used to switch or amplify voltage in circuits
* It is a current controlled device.
* It has 4 terminals
1) Soure 2) Gate 3) Drain 4. Body.

Types

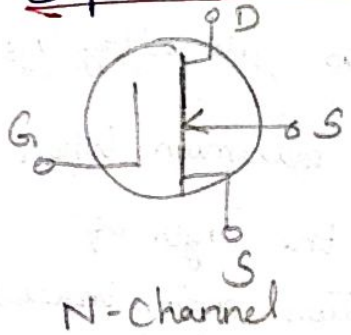


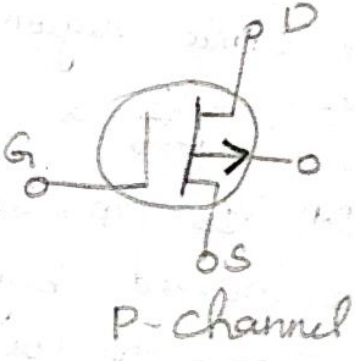
Enhancement MOSFET:





Depletion MOSFET

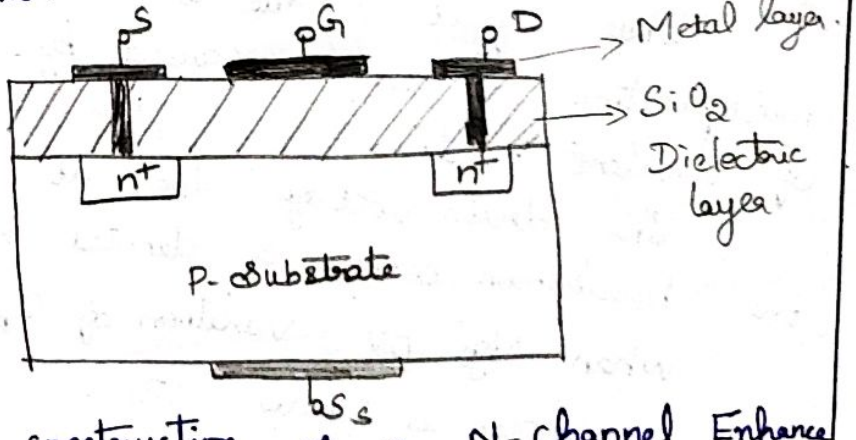




Enhancement MOSFET:

Construction:

The construction of an N-channel Enhancement MOSFET is shown in fig.



The construction of a N-channel Enhance MOSFET is shown in fig.

As there is no channel in E-MOSFET, the symbol is represented by the break line in the symbole.

Two heavily doped N^+ regions are diffused in lightly doped substrate of P-type silicon substrate D N^+ region is called the Source (S) and the other is called Drain (D).

A thin insulating layer of SiO_2 is grown over the surface of the structure and holes are cut into the oxide layer, allowing contact with source and drain

Then a thin layer of metal aluminium is formed over the layer of SiO_2. This metal layer covers the entire channel region and it forms the gate (G).

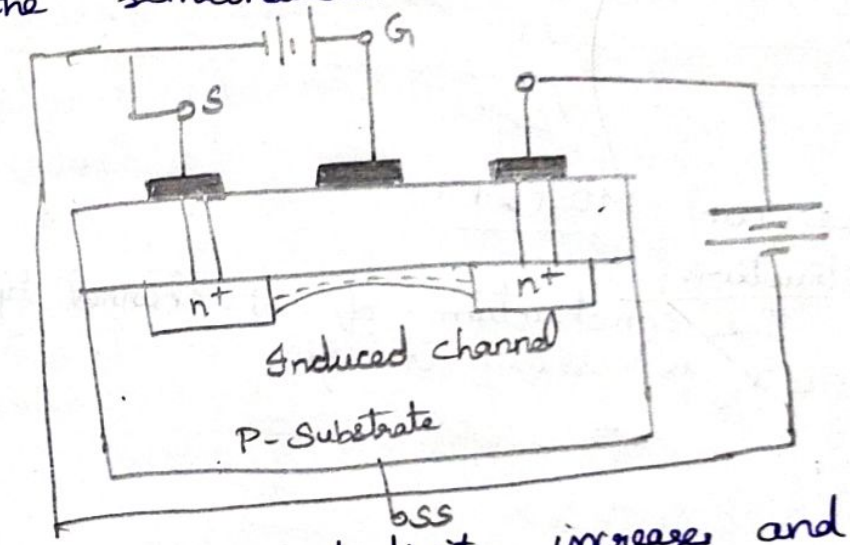
Operation :

The substrate and source are grounded and positive voltage is applied at the gate.

The positive charge on gate induces an equal negative charge on the substrate side between source and drain region.

The path is created between source and drain regions. The negative charge of electrons ~~or~~ which are minority carriers in the P-type substrate forms an inversion layer.

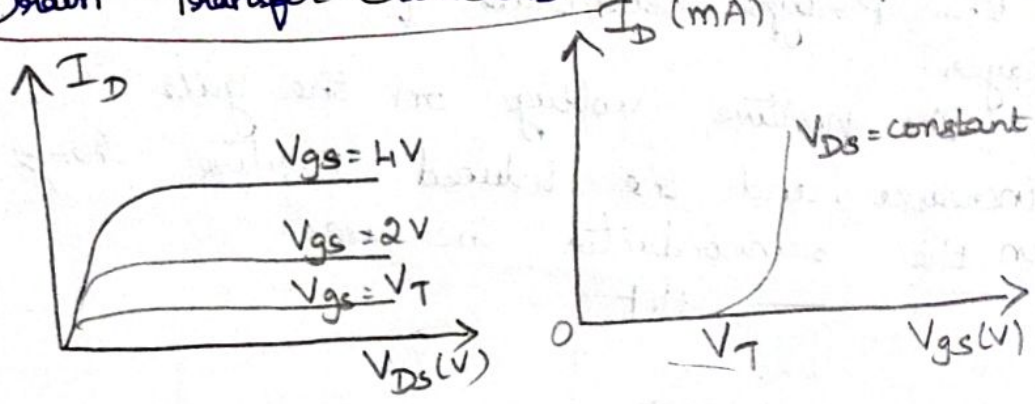
The positive voltage on the gate increases, and the induced negative charge on the semiconductor increases.



Hence, the conductivity increases and current flows from source to drain through the induced channel.

The drain current is enhanced by the positive gate voltage as in graphs.

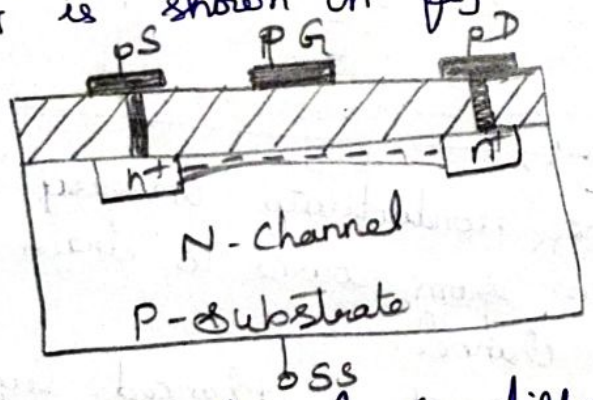
Drain Transfer Characteristics



DEPLETION MOSFET:

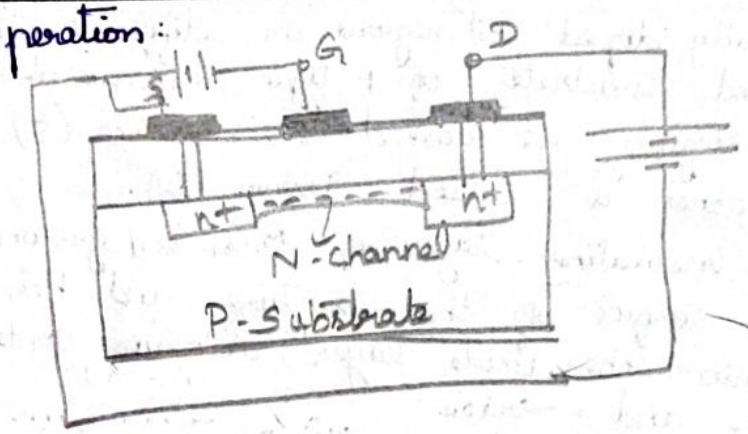
Construction:

The construction of N-channel depletion MOSFET is shown in fig.



When N-channel is diffused between the source and drain to the basic structure of Depletion MOSFET.

Operation:



When $V_{GS} = 0$;

The drain is positive w.r.t source the current flow (I_D) from source to drain through N-channel.

When $V_{GS} = -1V, -2V, \ldots$:

The drain to source current flow is reduced, since the N-channel width is reduced.

When $V_{GS} = V_{GS(OFF)}$:

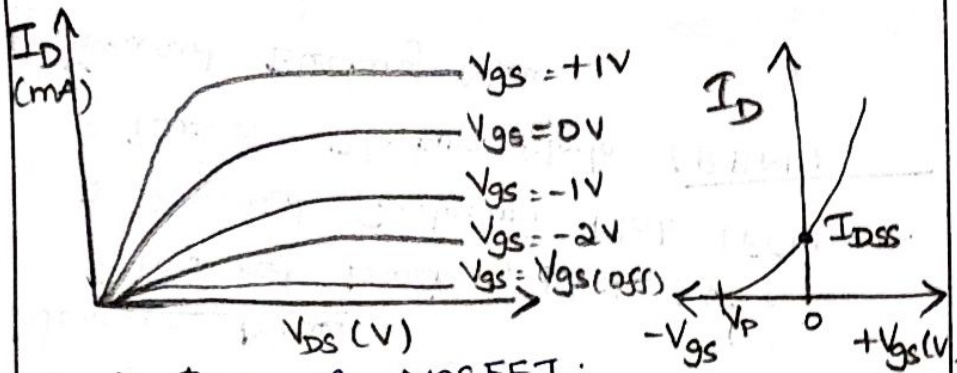
Between Source to drain the N-channel width becomes zero. So no I_D flows.

When $V_{gs} = +V, +2V, \ldots$

When V_{gs} is positive voltage, this induces the increase the N-channel width between source to drain. So current flows

through N-channel is also more. This is called Enhancement mode.

Drain Transfer Characteristics:

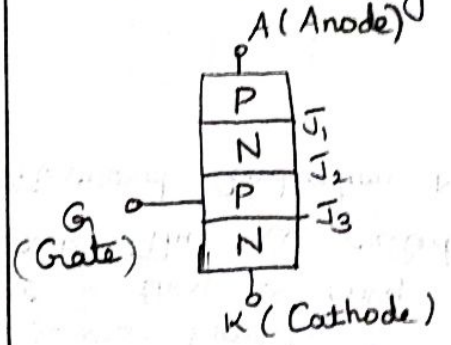


Applications of MOSFET:

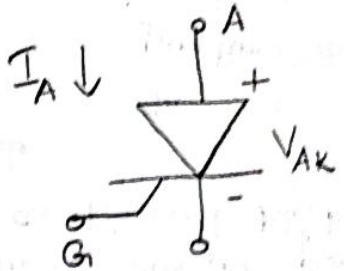
1) Used as amplifier in radio frequency (RF) applications.
2) Used as passive element like resistor (R), Capacitor (C) & Inductor (L)
3) Used as Power Regulators
4) Used as High speed switch
5) Used as Electronic DC relay

SILICON CONTROLLED RECTIFIER (SCR)

* A Silicon Controlled Rectifier is a four layer solid state current controlling device.
* It is also called as Semiconductor Controlled Rectifier.
* SCRs are available from few voltages to several KV and few amperes to several KA.
* It is a unidirectional device.
* It is a bipolar device (both electrons & holes are charge carriers).



a) Structure of SCR

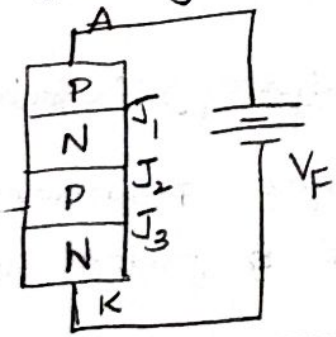


b) Symbol of SCR

* It is a 4 layer PNPN switching device with alternate layers of P & N semiconductor materials.
* It converts the AC signal to DC signal in controlled manner.
* For current conduction, J_1, J_2, J_3 must be forward biased.

Working Modes:
1. Forward Blocking Mode (FBM)
2. Forward Conduction Mode (FCM)
3. Reverse Blocking Mode (RBM)

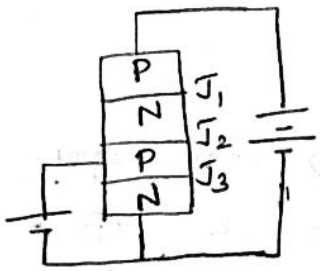
1) Forward Blocking Mode:



$J_1 \rightarrow F.B$
$J_2 \rightarrow R.B$
$J_3 \rightarrow F.B$

* J_1 & J_3 are forward biased, whereas J_2 is reverse biased.
* So there is only small current flowing through SCR. This is called as Forward blocking mode.

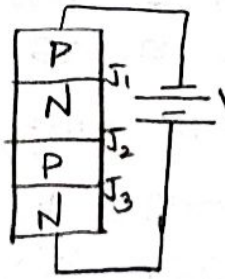
2) Forward Conduction Mode:



$J_1 \rightarrow F.B$
$J_2 \rightarrow F.B$
$J_3 \rightarrow F.B$

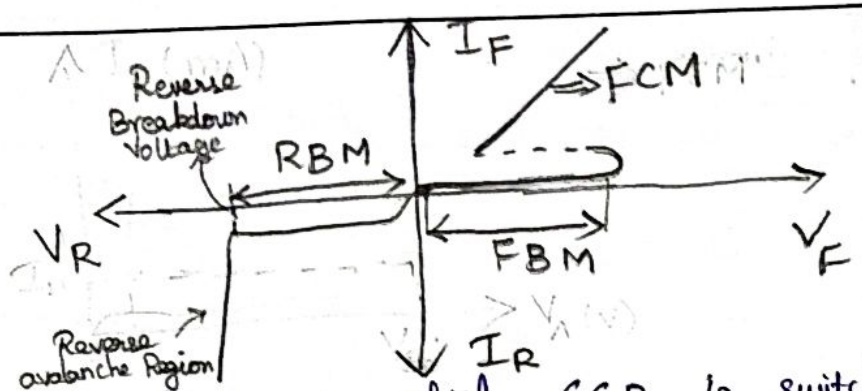
In this, the three junctions are forward biased. Hence the forward voltage drops and current starts to increase linearly.

3) Reverse Blocking Mode:



$J_1 \rightarrow R.B$
$J_2 \rightarrow F.B$
$J_3 \rightarrow R.B$

In this, J_1 & J_3 are reverse biased. When V_R voltage is increased there is small amount of current flow. At one level, there is junctional breakdown and the current starts to increase rapidly.



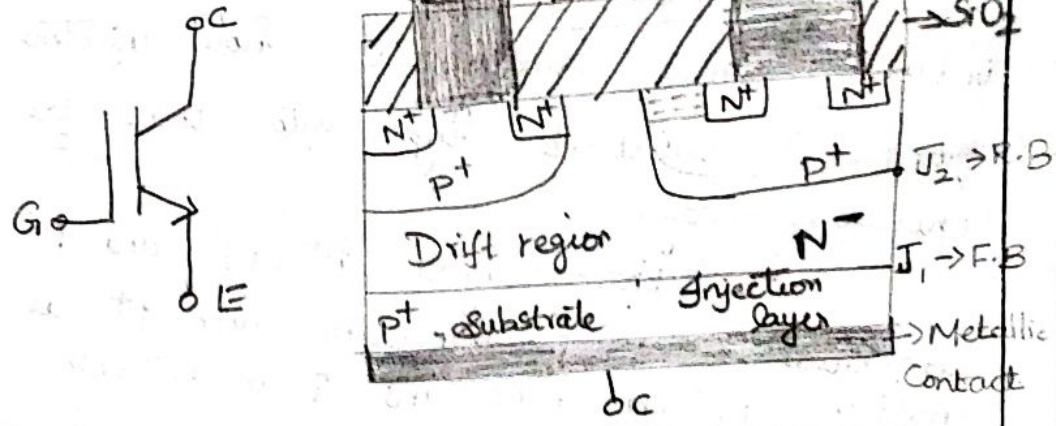
The voltage at which SCR is switched ON can be controlled by varying the gate current.

Applications of SCR

1.) Used in AC voltage stablizers.
2) Used as switch.
3) Used as choppers.
4) Used in inverter circuit.
5) Used in battery charger.
6) Used for speed controlled DC motor

INSULATED GATE BIPOLAR TRANSISTOR (IGBT):

* IGBT is a multi-layer semiconductor structure with alternate P-type and n-type doping.
* IGBT is combination of both power MOSFET and power BJT. (MOSFET → at i/p side, BJT → at o/p side)
* IGBT is also known as Metal Oxide Insulated Gate Transistor (MOSIGT), Conductively-Modulated Field Effect Transistor (COMFET), Gain Modulated FET (GMFET).



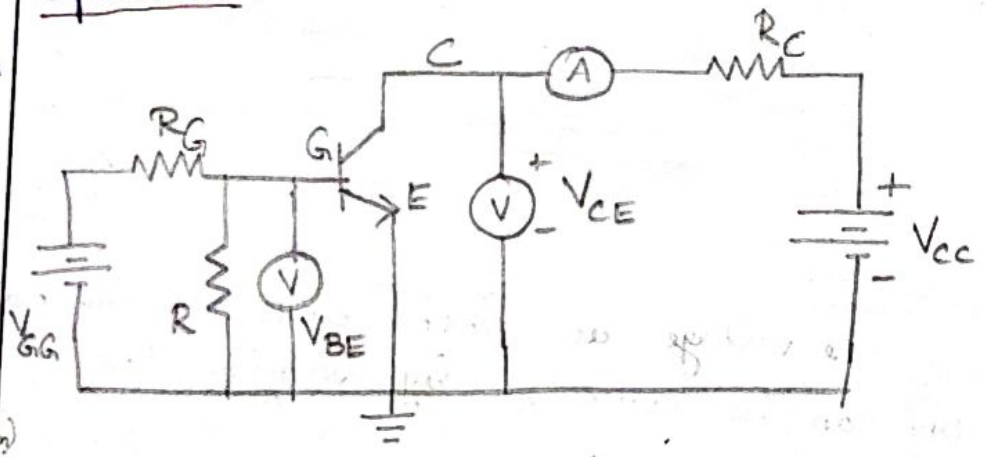
The N^+ layer substrate in drain is substituted in the IGBT by a P^+ layer substrate called collector.

When gate is positive with respect to emitter and emitter voltage greater than the threshold voltage of IGBT, a N-Channel is formed in the P-region as in power MOSFET. ($V_{GE} > V_T$, N-channel formed in P region)

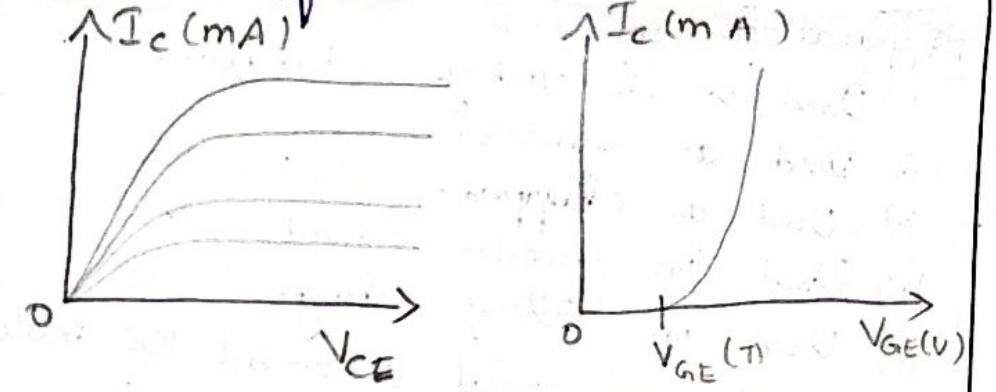
Thus N-channel short circuits the N^- region with N^+ emitter region. As electron movement in the N-channel intern, causes substantial hole injectors from P^+ substrate layer into that are epitaxial layer.

The three layers P^+, N^- and P^+ constitute a PNP transistor with p^+ as emitter, N^- as base and P as collector. Also P and N^+ layers constitute to NPN transistor.

Operation:



VI & Transfer Characteristics:



Static V-I characteristics of IGBT is shown in figure. The plot of collector current, (I_C) Vs collector emitter voltage, V_{CE} for various values of gate emitter voltage, V_{GE}.

The shape of the output characteristics is similar to that of BJT. But here the controlling parameter is gate emitter voltage (V_{GE}). Hence IGBT is voltage-controlled device.

The transfer characteristics of an IGBT is a plot of collector current (I_C) Vs Gate-emitter voltage (V_{GE}) as in figure. This characteristics is similar to power MOSFET.

When $V_{GE} < V_T$, IGBT is in the off state. When the device is off, junction J_2 blocks forward voltage and in case reverse voltage appears across collector and emitter junction, J_1 blocks it.

Applications of IGBT:

1) Used in SMPS
2) Used in UPS
3) Used for speed control of AC and DC motors.
* Used in inverters.
* Used in e-automobile system

INVERTER:

The inverter is an electronic circuit that converts fixed DC supply to variable AC supply.

The inverter is used to run the AC loads through a battery.

Types:

1. Single Phase Inverter
2. Three Phase Inverter

Single Phase Inverter:

The single phase inverter is also called as half bridge rectifier. It converts DC supply to single phase AC supply. For this purpose two switching devices (SCR, MOSFET, IGBT) are used to convert DC to AC. Diodes and

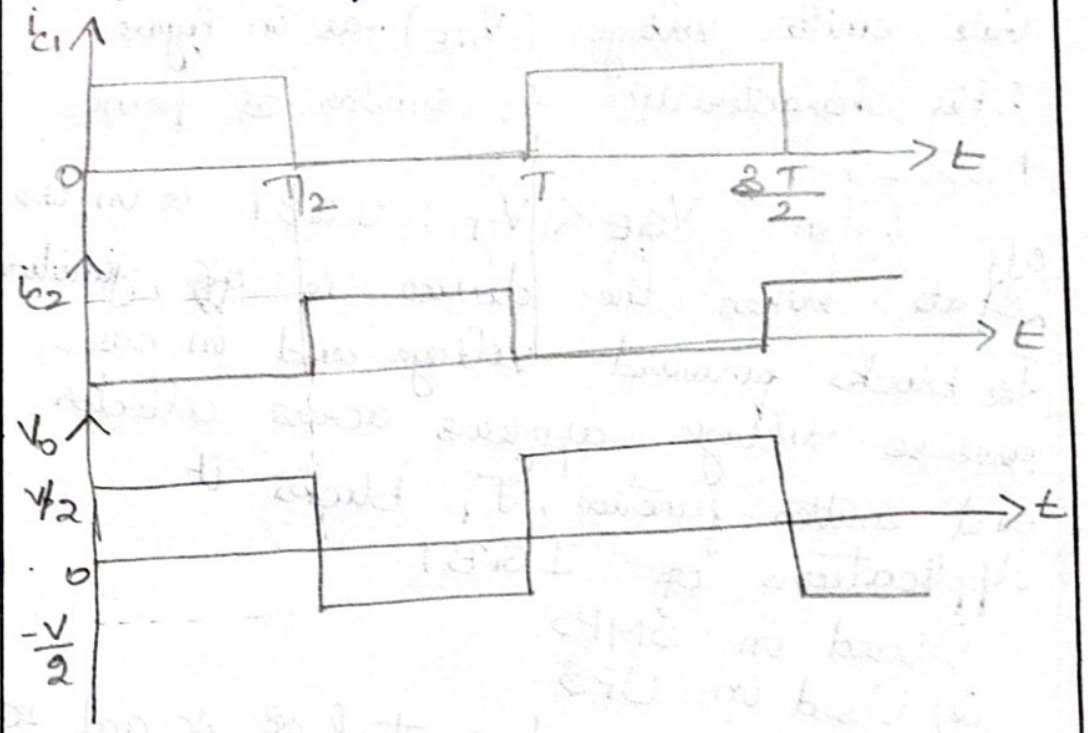
Capacitors helps the circuit to operate smoothly.

Working:

In the half bridge inverter, the output varies from $+\frac{V_s}{2}$ to $-\frac{V_s}{2}$. As shown in the circuit, two switching devices are connected in one common branch. The switching device may be SCR, MOSFET or IGBT.

Generally in inverter, MOSFET is commonly used as switching device. Two switches S_1 & S_2 are used. To obtain one cycle of alternating voltage each device is triggered at one time. The other being off at the same time. For example to obtain the positive cycle, of alternating supply, device S_1 is turned ON, while S_2 is kept OFF. Similarly to obtain negative cycle of alternating supply, device S_2 is turned ON while S_1 is kept off. The output wave is shown in figure.

Output Waveform:



As shown in the output waves, when S_1 is conducting from 0 to $\frac{T}{2}$, the output $+\frac{V_s}{2}$ is obtained. Similarly, the output $\frac{V_s}{2}$ is when S_2 is conducting from $\frac{T}{2}$ to T, the output $\frac{V_s}{2}$ is obtained. Hence the output alternates between $+\frac{V_s}{2}$ to $-\frac{V_s}{2}$, which is regarded as alternating voltage, T is the total time period of the conduction of two devices.

It can be noted that the output voltage waveform is a stepped square waveform.

In inverters the stepped square waveform alternates between two values, which is considered as alternating voltage

Applications :

1) Used in UPS
2) Used as speed control in DC motor
3) Used in High Voltage DC systems (HVDC).
4) Used in refrigeration compressors.
5) Used in solar power generation system.

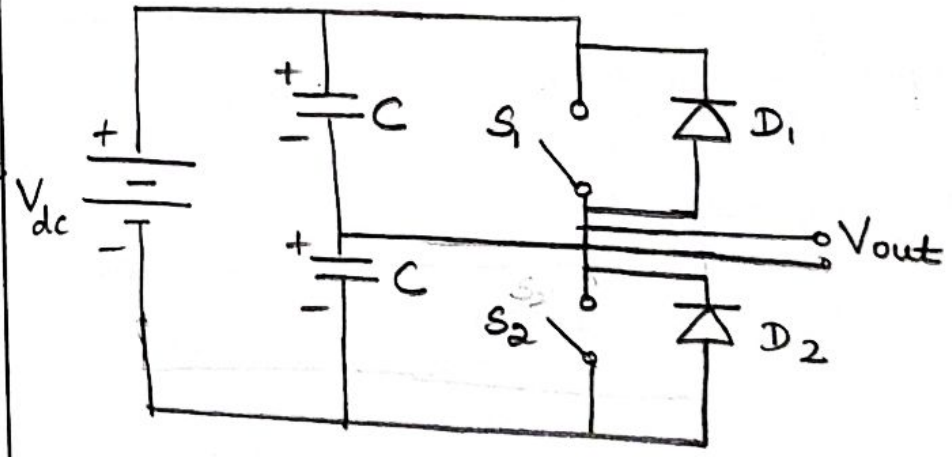


Fig: Single Phase Inverter

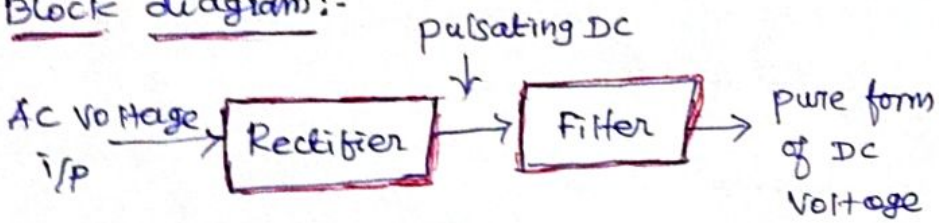
inverter.

DEPARTMENT OF

Rectifiers

* The Circuits which are used to Convert a.c voltage to d.c voltage are called 'Rectifiers'.

* Block diagram:-

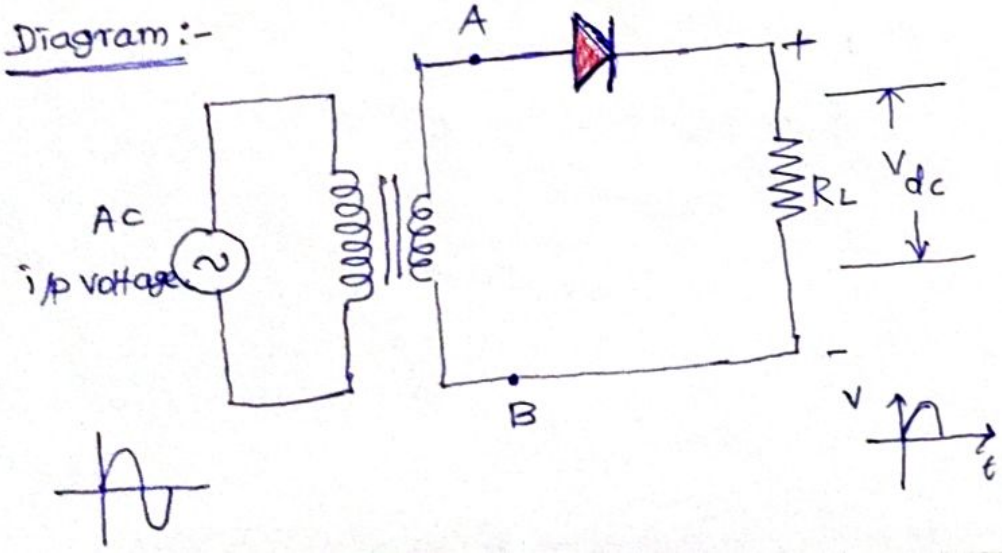


* Types:-

1. Half-wave Rectifier
2. Centre tapped full-wave rectifier
3. Full-wave bridge rectifier

Half-wave Rectifier:-

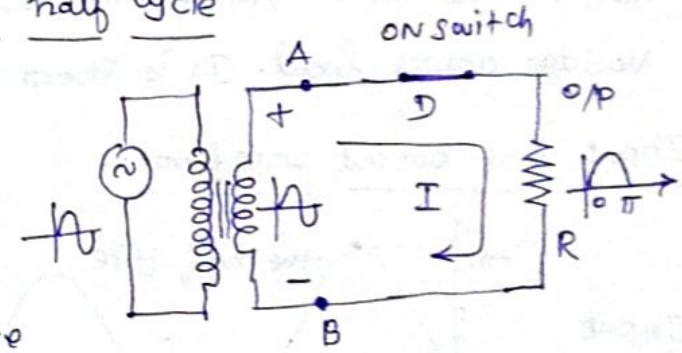
Diagram:-



* It Consists of transformer, diode and load resistance.
* Here, diode acts as a switch. i/e uder forward biasing condition, it is a closed switch, and reverse biasing condition, it is a open switch.
* The transformer used to step-down the a.c voltage (I/p voltage).

* Operation:-

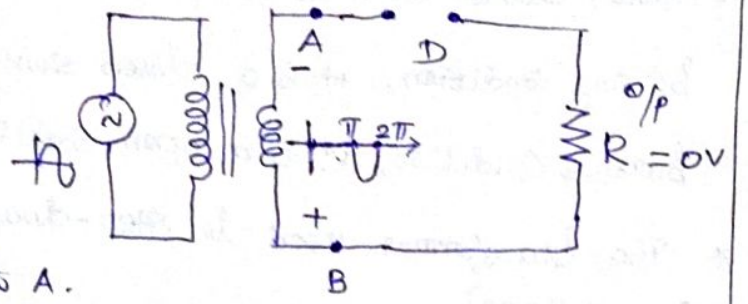
During +ve half cycle



* During +ve half-cycle of the input voltage (0 to π), the point 'A' is +ve with respect to point 'B'.
* During this period, the diode becomes forward biased and it acts as a (ON) closed switch.
* The entire positive input voltage is applied across the load. The current path is A-D-R-B. It is shown in figure above.

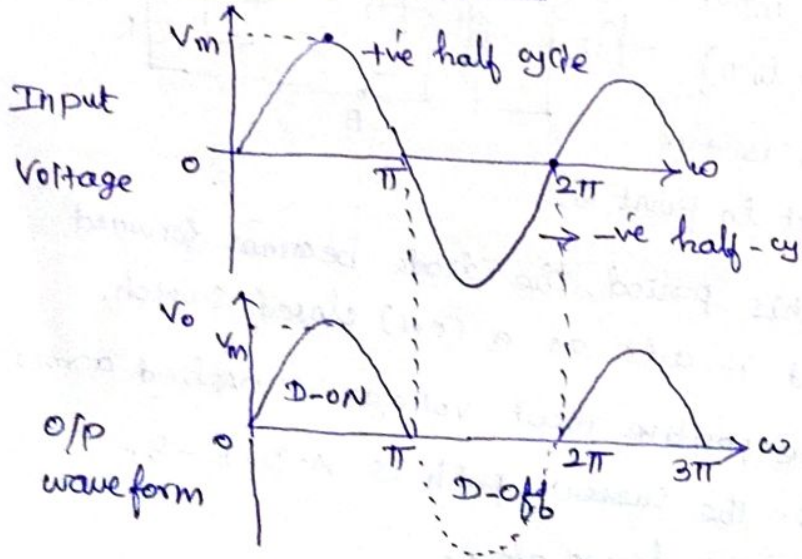
→ * During negative half cycle: (off) switch open circuite

* During this period ($\pi - 2\pi$), the point 'B' is positive with respect to A.



* In this period, Diode 'D' becomes reverse biased. Then it acts as a open switch. So, there is no o/p voltage across load. It is shown in above figure.

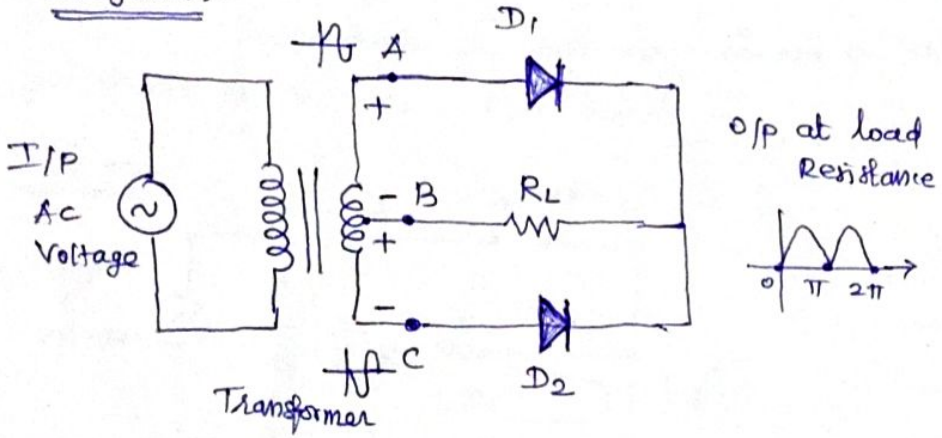
Input and output waveforms:-



During negative half cycle of the input voltage

II: Centre tapped Full-wave Rectifier

Diagram:-



* The fig, shows the centre tapped fullwave-rectifier Circuit.
* It consists of two diodes, one centre tapped trasformer and load resistance.
* By Centre tapping, the secondary winding is divided into two equal parts.
* Thus, the voltage available between A to B is 180° out of phase with the voltage available between B to C.

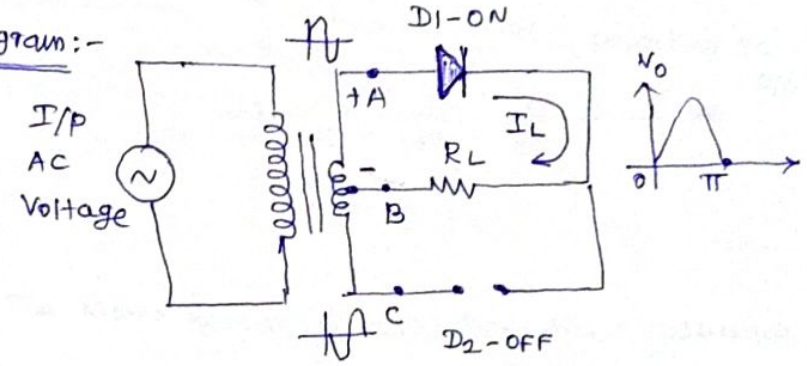
I/P at D2 Vin ↑

Operation:-

When an A.C voltage is applied to primary winding of transformer, as per the principle of transformer, it transfers the primary voltage into secondary voltage without changing its frequency.

* During positive half cycle:-

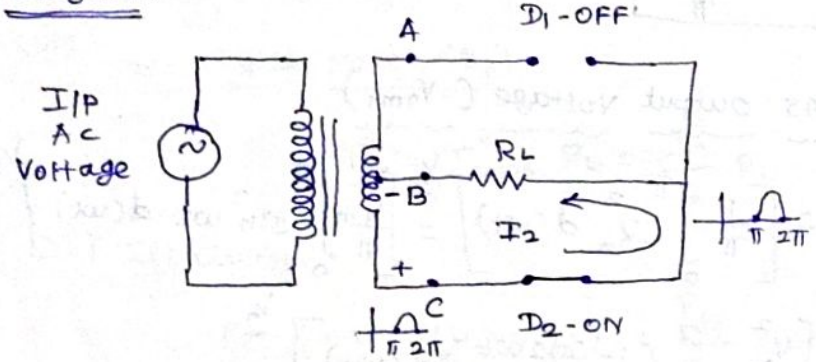
Diagram:-



* During positive half cycle of the input voltage, the terminal 'A' is more positive than terminal 'C'. Thus diode 'D1' becomes more forward biased than diode D_2.
* Thus, D_1 → acts as a closed switch, D_2 → acts as a Open switch. The current path is A - D_1 - R_L - B
* Therefore, we can get positive output voltage across load. It is shown in below fig.

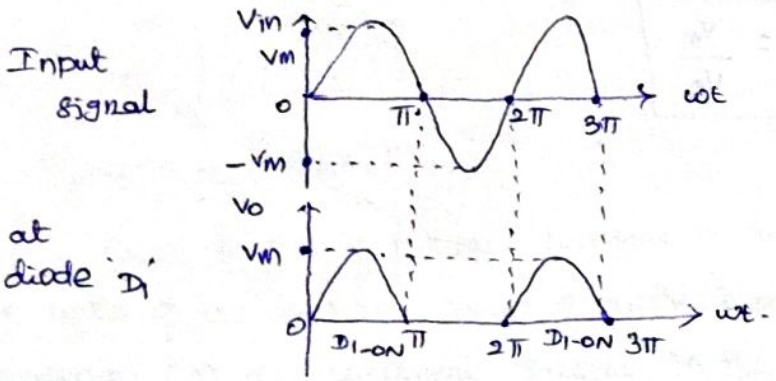
During negative half cycle of the input voltage, the terminal 'C' is more positive than terminal 'A'. Thus, diode 'D_2' becomes more forward biased than diode D_1. Thus, diode D_2 acts as a closed switch and diode D_1 acts as a open switch.

Diagram:-

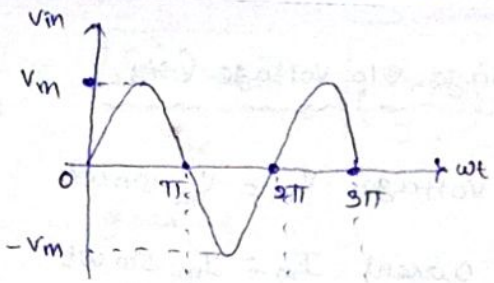


* Then the current path is C – D_2 – R_L – B. Here, we can get positive output voltage across load. It is shown in below fig.

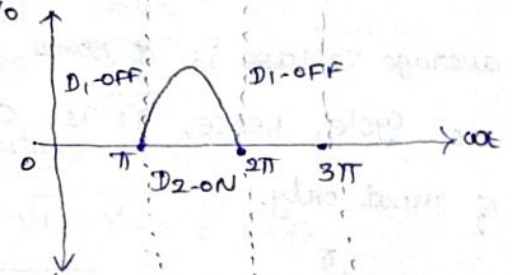
I/p & o/p waveforms.



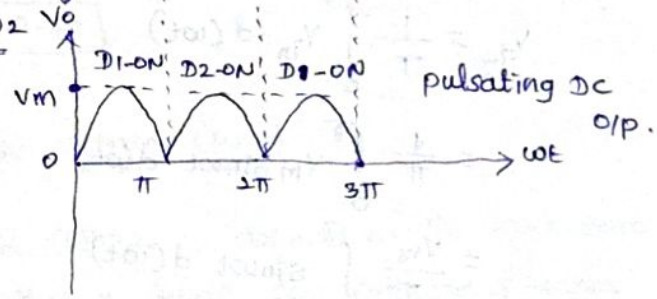
I/p at 'D_2'



o/p at 'D_2'



Final o/p at D_1 & D_2



pulsating DC o/p.

Note:-

The Ripple frequency on a single phase full-wave rectifier is twice the supply frequency. i.e 2f.

* If the supply frequency is 50 Hz, the ripple frequency of this rectifier is 2×50 = 100 Hz.

* (i) Average o/p voltage (V_{dc})

Input voltage $V_{in} = V_m \sin\omega t$

Input current $I_{in} = I_m \sin\omega t$

DC (or) average voltage is of same form in the two half of the ac cycle. Hence, it is calculated for half cycle of input only.

$$V_{dc} = \frac{1}{T}\int_0^{\pi} V_{in}\, d(\omega t)$$

$$= \frac{1}{\pi}\int_0^{\pi} V_m \sin\omega t\, d(\omega t)$$

$$= \frac{V_m}{\pi}\int_0^{\pi} \sin\omega t\, d(\omega t)$$

$$= \frac{V_m}{\pi}(-\cos\omega t)_0^{\pi} = \frac{V_m}{\pi}[-\cos\pi - (-\cos 0)]$$

$$V_{dc} = \frac{V_m}{\pi}[1+1] = \frac{2V_m}{\pi}$$

$$\boxed{V_{dc} = \frac{2V_m}{\pi}}$$

(ii) Average input current (I_{dc})

$$I_{dc} = \frac{1}{T}\int_0^{T} I_{in}\, d(\omega t)$$

$$= \frac{1}{\pi}\int_0^{\pi} I_m \sin\omega t\, (d(\omega t))$$

$$\boxed{I_{dc} = \frac{2I_m}{\pi}}$$

(iii) RMS output voltage (V_{rms})

$$V_{rms} = \left[\frac{1}{\pi}\int_0^{\pi} V_{in}^2\, d(\omega t)\right]^{1/2} = \left[\frac{V_{in}^2}{\pi}\int_0^{\pi} \sin^2\omega t\, d(\omega t)\right]^{1/2}$$

$$= \left[\frac{V_m^2}{\pi}\int_0^{\pi}\left(\frac{1-\cos 2\omega t}{2}\right) d(\omega t)\right]^{1/2}$$

$$= \left[\frac{V_m^2}{\pi}\left(\omega t - \frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]^{1/2}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

(iv) RMS output current :- (I_{orms})

$$I_{orms} = \frac{V_{orms}}{R_L} = \frac{V_M}{\sqrt{2}\cdot R_L} = \frac{I_m}{\sqrt{2}} \qquad \left(\because I_m = \frac{V_m}{R_L}\right)$$

(v) Dc output power :- (P_{dc})

$$P_{dc} = I_{dc}^2 R_L = \frac{4 I_m^2}{\pi^2}\cdot R_L$$

(vi) Ac Input power (P_{in})

$$P_{in} = I_{orms}^2 \cdot R_L = \frac{I_m^2}{2}\cdot R_L$$

(vii) Efficiency.

$$\text{Rectifier efficiency } (\eta) = \frac{P_{dc}}{P_{ac}} \times 100$$

$$= \frac{\frac{4I_m^2}{\pi^2}\cdot R_L}{\frac{I_m^2}{2}\cdot R_L} = \frac{8}{\pi^2} \times 100$$

$$\boxed{\eta = 81\%}$$

(viii) Ripple factor (RF)

Ripple factor of fullwave rectifier is defined as the ratio of ac (or) rms value of ripple component to average (or) dc component present in the output.

$$RF = \frac{I_{orms}}{I_{dc}} = \frac{\sqrt{I_{orms}^2 - I_{dc}^2}}{I_{dc}} = \sqrt{\left(\frac{I_{orms}}{I_{dc}}\right)^2 - 1}$$

The form factor is given by,

$$FF = \frac{I_{orms}}{I_{dc}} = \frac{I_m/\sqrt{2}}{\frac{2I_m}{\pi}} = \frac{\pi}{2\sqrt{2}} = 1.11$$

Hence, Ripple Factor,

$$RF = \sqrt{(1.11)^2 - 1} = 0.48$$

$$\boxed{RF = 0.48}$$

(ix) Peak-Inverse Voltage (PIV)

Peak inverse voltage is defined as the maximum (or) peak voltage that a diode can withstand under reverse biased condition.

PIV- calculated as follows:-

Assume, positive half cycle of input, D_1 is Conduction and D_2 is off. The maximum voltage is V_m droped at R_L. similarly for negative half cycle, D_1 is OFF, D_2 is ON. So o/p is again V_m.

So $\boxed{PIV = V_m + V_m = 2V_m}$

(x) Transformer utilization factor (TUF):

In this case, TUF is found by considering primary and secondary VA rating separately and take the average of two halves.

TUF for secondary (or) secondary utilisation factor SUF can be calculated as,

$$SUF = (TUF)_s = \frac{P_{dc}}{P_{ac\ rated}}$$

$$= \frac{I_{dc}^2 \cdot R_L}{V_{0rms} \cdot I_{0rms}} = \frac{\left(\frac{2I_m}{\pi}\right)^2 \cdot R_L}{\frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}} = \frac{\left(\frac{2I_m}{\pi}\right)^2 \cdot R_L}{\frac{I_m \cdot I_m \cdot R_L}{2}}$$

$$= \frac{4I_m^2/\pi^2}{I_m^2/2} = \frac{8}{\pi^2} \times 100 = 81.1\%$$

$$SUF = (TUF)_s = 81.1\%$$

Transformer primary supplies input for both half cycle of input, thus,

TUF for primary $= (TUF)_p$

$= 2 \times 28.87\% = 57.2\%$

$$\%\ TUF = \frac{(TUF)_p + (TUF)_s}{2} = 69.15\%$$

Advantages:-

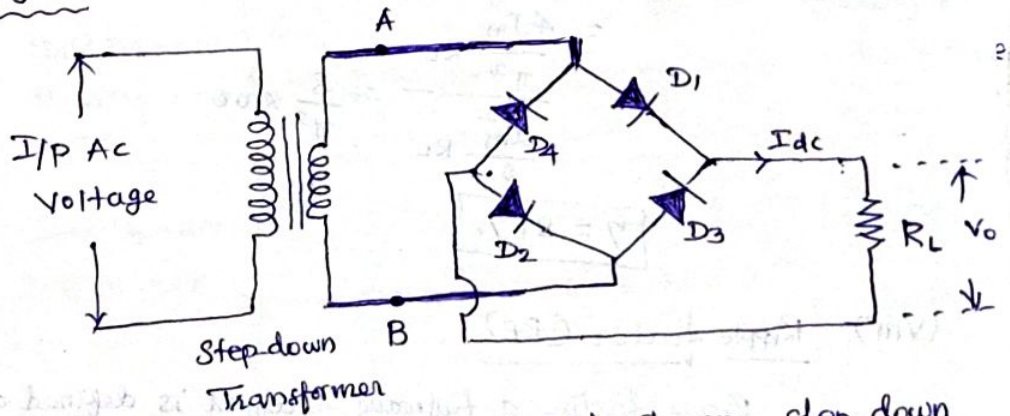
1. The output voltage and transformer efficiency are high.
2. Low ripple factor
3. High transformer utilisation factor.

Dis-advantages:-

1. Usage of additional diode and bulky transformer is needed, and hence increase in cost
2. The peak inverse voltage of diode is high ($2V_m$).

FULL WAVE BRIDGE RECTIFIER

Diagram:-

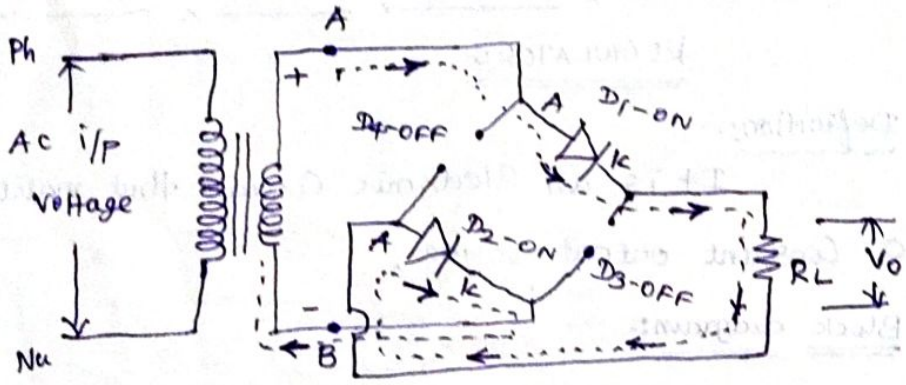


* Bridge rectifier diagram consists of one-step down transformer, 4-pn-Junction diode, and one load resistor (R_L).

Operation:-

* During the positive half cycle of the input voltage, the terminal 'A' is positive with respect to 'B'. Thus, diodes D_1 & D_2 are in forward biasing and D_3 & D_4 are in reverse biasing.

* Then the current flow is shown in below fig.

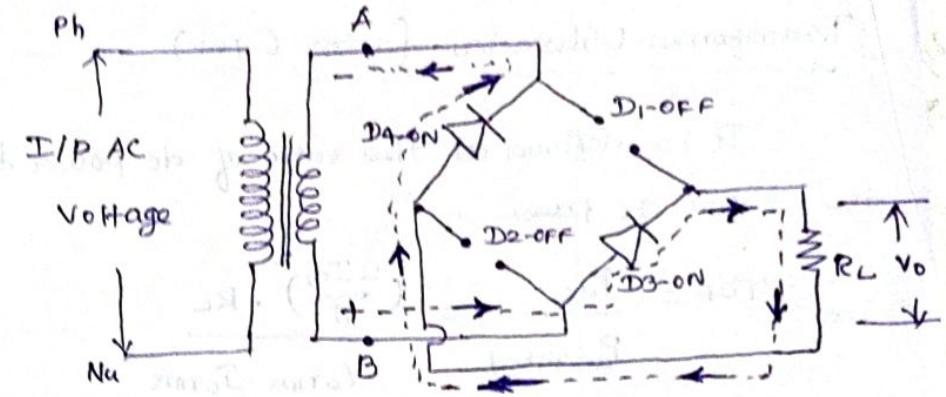


* During negative half cycle of the input voltage, the terminal 'B' is positive with respect to 'A'.

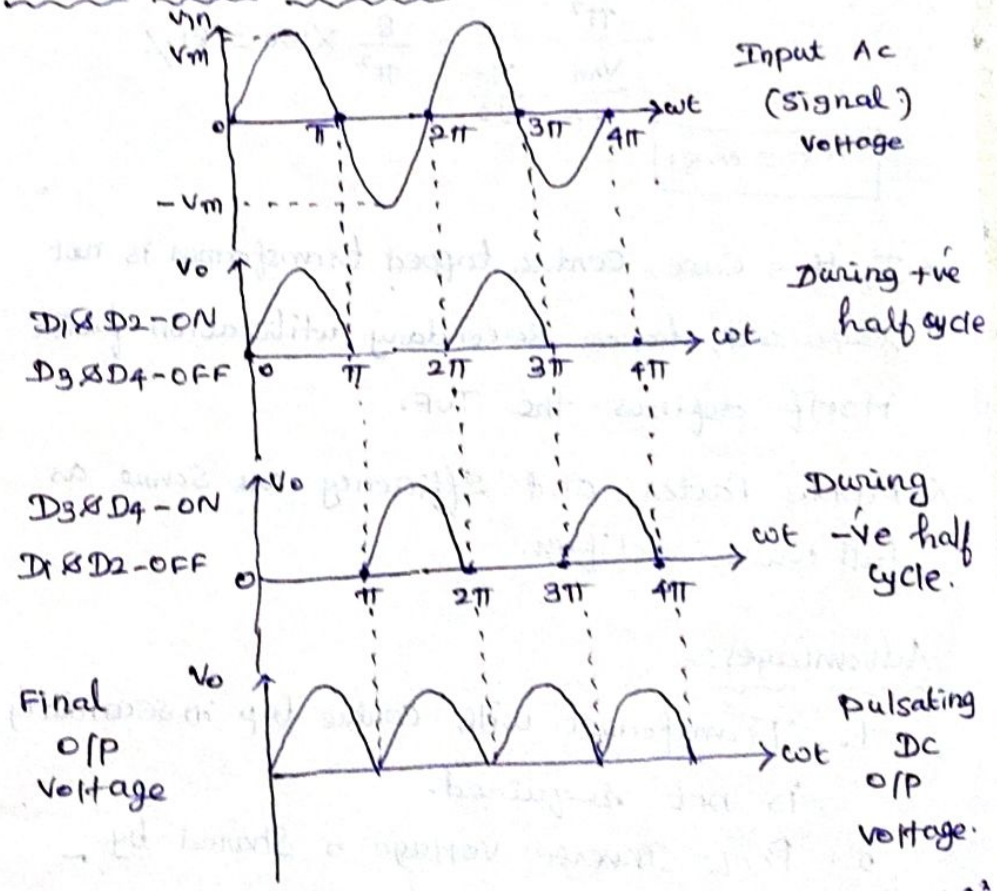
* Thus, diodes D_3 and D_4 are forward biased and diodes D_1 and D_2 are reverse biased.

* The current path is B - D_3 - R_L - D_4 - A.

* It is shown in below fig.



Input & output waveforms:-



Transformer Utilisation factor (TUF)

It is defined as the ratio of dc power to the rated ac power.

$$\text{i.e } TUF = \frac{P_{dc}}{P_{ac\ rated}} = \frac{\left(\frac{2I_m}{\pi}\right)^2 \cdot R_L}{V_{0rms} \cdot I_{0rms}}$$

$$= \frac{\frac{4I_m^2}{\pi^2} \cdot R_L}{\frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}} = \frac{8}{\pi^2} \times 100 = 81\%$$

TUF = 0.81

* In this case, centre tapped transformer is not required, hence secondary utilization factor itself defines the TUF.
* Ripple Factor and Efficiency are same as full wave rectifier.

Advantages:-

1. Transformer with centre tap in secondary is not required.
2. Peak Inverse voltage is shared by D_1, D_2 and D_3, D_4 combinations equivally.
3. Better transformer utilization factor.

Dis-advantages:-

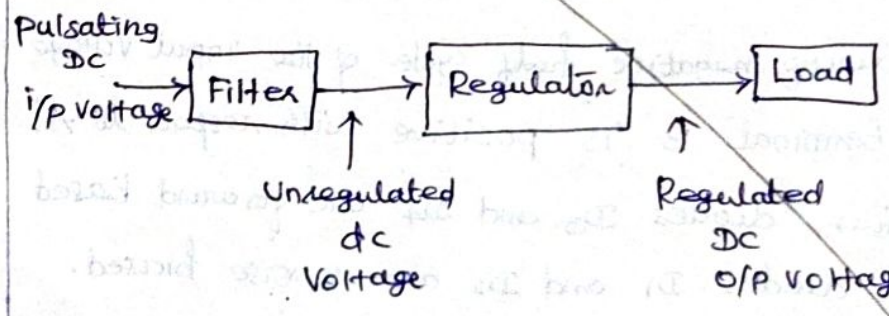
1. Additional 2-diodes are required.
2. Efficiency is slightly reduced than the FWR.

REGULATORS

Definition:-

It is an Electronic Circuit that maintains a constant output voltage.

Block diagram:-



The reverse voltage appearing across the reverse biased diodes is $2V_m$ but two diodes are sharing it.

Hence PIV rating of the diode is V_m and not $2V_m$ as in case of full wave rectifier

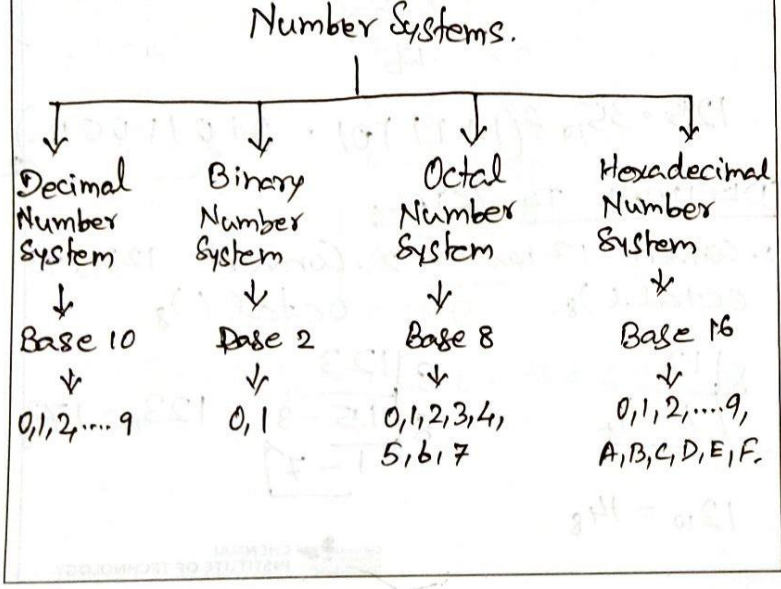
3.26. COMPARISON OF HWR, FWR & BRIDGE RECTIFIER

Parameter	Half wave Rectifier	Full wave Rectifier	Bridge Rectifier
No. of diodes	One	Two	Four
Ripple Frequency	f_s	$2\ f_s$	$2f_s$
PIV	V_m	$2\ V_m$	V_m
I_m	$\frac{V_m}{R_f + R_L}$	$\frac{V_m}{R_f + R_L}$	$\frac{V_m}{2R_f + R_L}$
Average current (I_{dc})	I_m/π	$2I_m/\pi$	$2I_m/\pi$
RMS value	$I_m/2$	$I_m/\sqrt{2}$	$I_m/\sqrt{2}$
DC value (V_{DC})	$\frac{V_m}{\pi} - I_{dc}R_f$	$\frac{2V_m}{\pi} - I_{dc}R_f$	$\frac{2V_m}{\pi} - 2I_{dc}R_f$
Ripple factor	1.21	0.482	0.482
P_{DC}	$I_{dc}^2 R_L$	$I_{dc}^2 R_L$	$I_{dc}^2 R_L$
P_{AC}	$I_{RMS}^2 (R_f + R_L)$	$I_{RMS}^2 (R_f + R_L)$	$I_{RMS}^2 (2R_f + R_L)$
Efficiency (η)	40.5%	81.0%	81.0%
TUF	0.286	0.692	0.812

UNIT-IV DIGITAL ELECTRONICS.

Review of number systems, binary codes, error detection and correction codes, combinational logic - representation of logic functions - SOP and POS forms, K-map representations - minimization using K-maps (Simple problems only).

REVIEW OF NUMBER SYSTEMS.



Decimal	Binary	Octal	Hexadecimal
0	0	0	0
1	1	1	1
2	10	2	2
3	11	3	3
4	100	4	4
5	101	5	5
6	110	6	6
7	111	7	7
8	1000	10	8
9	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F

NUMBER CONVERSIONS.

DECIMAL TO BINARY

1. Convert 43_{10} to Binary.

2 | 43	
2 | 21	- 1
2 | 10	- 1
2 | 5	- 0
2 | 2	- 1
	1 - 0

$43_{10} = 101011_2$

2. Convert 13_{10} to Binary

2 | 13	
2 | 6	- 1
2 | 3	- 0
	1 - 1

$13_{10} = 1101_2$

3. Convert 12.25_{10} to Binary.

2 | 12	
2 | 6	- 0
2 | 3	- 0
	1 - 1

0.25×2
0.50×2
1.00

$12.25_{10} = 1100.01_2$

4. Convert 125.35_{10} to Binary.

2 | 125	
2 | 62	- 1
2 | 31	- 0
2 | 15	- 1
2 | 7	- 1
2 | 3	- 1
	1 - 1

0.35×2
0.70×2
1.40×2
0.80×2
1.60×2
1.20×2
0.40×2
0.80×2
1.60

$125.35_{10} = (1111101.0101100\ldots)_2$

DECIMAL TO OCTAL.

1. Convert 12_{10} to Octal.$()_8$.

8 | 12	
	1 - 4

$12_{10} = 14_8$

2. Convert 123_{10} to Octal $()_8$.

8 | 123	
8 | 15	- 3
	1 - 7

$123_{10} = 173_8$

3. Convert 45.96_{10} to Octal $()_8$.

$8 \mid 45$
$5 - 5$ ↑

0.96×8
7.68×8
3.84×8
7.62 ↓

$(45.96)_{10} = (55.737\ldots)_8$.

4. Convert $(158.45)_{10}$ to octal $()_8$.

$8 \mid 158$
$8 \mid 19 - 6$
$2 - 3$ ↑

0.45×8
3.60×8
4.80×8
6.40×8
3.20×8
1.60 ↓

$(158.45)_{10} = (236.34631\ldots)_8$

DECIMAL TO HEXADECIMAL.

1. Convert 125_{10} to Hexadecimal $()_{16}$.

$16 \mid 125$
$7 - (13) - D$

$125_{10} = 7D_{16}$

2. Convert 450_{10} to Hexadecimal $()_{16}$.

$16 \mid 450$
$16 \mid 28 - 2$
$1 - (12) - C$

$450_{10} = 1C2_{16}$

3. Convert 157.25_{10} to Hexadecimal $()_{16}$.

$16 \mid 157$
$9 - (13) D$

0.25×16
4.00 ←

$157.25_{10} = 9D.4_{16}$

4. Convert 255.132_{10} to Hexadecimal $()_{16}$.

$16 \mid 255$
$15 - (15) - F$
F

0.132×16
2.112×16
1.792×16
12.672
C ←

$(255.132)_{10} = (FF.21C\ldots)_{16}$

BINARY TO DECIMAL

1. Convert 1011_2 to Decimal $()_{10}$.

$1 \times 2^0 = 1$
$1 \times 2^1 = 2$
$0 \times 2^2 = 0$
$1 \times 2^3 = 8$
11_{10}

$1011_2 = 11_{10}$

2. Convert 10110_2 to Decimal $()_{10}$.

$0 \times 2^0 = 0$
$1 \times 2^1 = 2$
$1 \times 2^2 = 4$
$0 \times 2^3 = 0$
$1 \times 2^4 = 16$
22

$10110_2 = 22_{10}$.

3. Convert 111.01_2 to Decimal $()_{10}$.

$1 \times 2^0 = 1$
$1 \times 2^1 = 2$
$1 \times 2^2 = 4$
7

0.01
$1 \times 2^{-2} = 0.25$
$0 \times 2^{-1} = 0$
0.25

$111.01_2 = 7.25_{10}$

4. Convert 1010.101_2 to Decemal $()_{10}$.

1010
$0 \times 2^0 = 0$
$1 \times 2^1 = 2$
$0 \times 2^2 = 0$
$1 \times 2^3 = 8$
10

0.101
$1 \times 2^{-3} = 0.125$
$0 \times 2^{-2} = 0$
$1 \times 2^{-1} = 0.5$
0.625

$(1010.101)_2 = (10.625)_{10}$

OCTAL TO DECIMAL

1. convert 123_8 to Decimal $()_{10}$.

$3 \times 8^0 = 3$
$2 \times 8^1 = 16$
$1 \times 8^2 = 64$
83

$123_8 = 83_{10}$

2. Convert 765_8 to Decimal $()_{10}$.

$5 \times 8^0 = 5$
$6 \times 8^1 = 48$
$7 \times 8^2 = 448$
501

$765_8 = 501_{10}$

3. Convert 123.45_8 in to Decimal $(\ )_{10}$

123
- $3 \times 8^0 = 3$
- $2 \times 8^1 = 16$
- $1 \times 8^2 = 64$

83

0.45
- $5 \times 8^{-2} = 0.078$
- $4 \times 8^{-1} = 0.5$

0.578

$123.45_8 = 83.578125_{10}$

4. Convert 77.22_8 into Decimal $(\ )_{10}$.

77
- $7 \times 8^0 = 7$
- $7 \times 8^1 = 56$

63

0.22
- $2 \times 8^{-2} = 0.03125$
- $2 \times 8^{-1} = 0.25$

0.28125

~~$77.22_8 = 6360.28125_{10}$~~.

$77.22_8 = 63.28125_{10}$.

HEXADECIMAL TO DECIMAL

1. Convert $A2_{16}$ in Decimal $(\ )_{10}$.

A 2
- $2 \times 16^0 = 2$
- $A(10) \times 16^1 = 160$

162

$A2_{16} = 162_{10}$

2. Convert $C5_{16}$ into Decimal $(\ )_{10}$

C 5
- $5 \times 16^0 = 5$
- $C(12) \times 16^1 = 192$

197

$C5_{16} = 197_{10}$

3. Convert $1B.12_{16}$ into $(\ )_{10}$

1B
- $B(11) \times 16^0 = 11$
- $1 \times 16^1 = 16$

27

0.12
- $2 \times 16^{-2} = 0.0078125$
- $1 \times 16^{-1} = 0.0625$

0.0703125

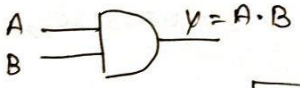
$1B.12_{16} = 27.0703125_{10}$

BINARY CODES.

Decimal	BCD 8421	2421	Excess-3
0	0000	0000	0011
1	0001	0001	0100
2	0010	0010	0101
3	0011	0011	0110
4	0100	0100	0111
5	0101	1011	1000
6	0110	1100	1001
7	0111	1101	1010
8	1000	1110	1011
9	1001	1111	1100

LOGIC GATES.

AND GATE

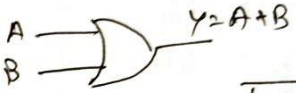


* If both the inputs are logic one (High), then output is logic one (High).

A	B	Y=A·B
0	0	0
0	1	0
1	0	0
1	1	1

* If any one of the input is logic zero (low), then, output is logic zero (low).

OR GATE.

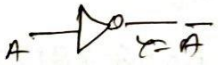


* If any one of the inputs are is logic one (High), then, output is logic one (High).

A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

* If both the inputs are logic zero (low), then, output is logic zero (low).

NOT GATE.

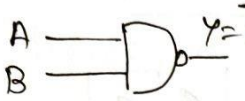


* If input is logic zero, then, output is logic one.

A	Y=Ā
0	1
1	0

* If input is logic one (High), then, output is logic zero (low).

NAND GATE.



A	B	$Y=\overline{A\cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

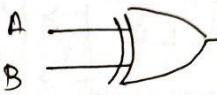
* If any one of the input is logic zero(low), then, output is logic one (High).
* If both the inputs are logic one(High), then, output is logic zero (low).

NOR GATE.

A	B	$Y=\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

* If both the inputs are logic zero (low), then, output is logic one(High).
* If any one of the ~~output~~ is logic one(High), then, output is logic zero(low).

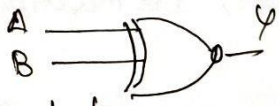
EX-OR (EXCLUSIVE OR) GATE



A	B	$Y=A\oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

* If both the inputs are different, then, output is logic one(High).
* If both the inputs are same, then, output is logic zero(low).

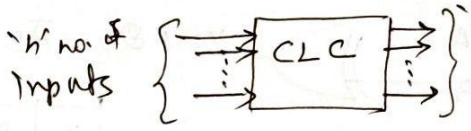
EX-NOR GATE.



A	B	$Y=A\odot B$
0	0	1
0	1	0
1	0	0
1	1	1

* If the both the inputs are same, then the output is logic one(High).
* If both the inputs are different, then, output is logic zero (low).

COMBINATIONAL LOGIC CIRCUITS.



The logic circuits, whose outputs at any instant of time are entirely depedent upon the input signals present at that time are known as combinational logic circuits.

Eg. Adder, Substractor, Decoder, Encoder, Multiplexer, Demultiplexer.

ADDERS.

HALF ADDER: A combinational circuit that performs the addition of two bits is called half adder.

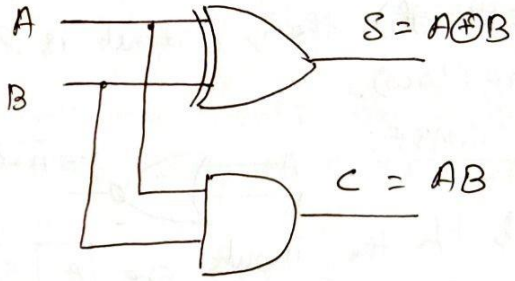
FULL ADDER. A circuit that performs addition of three bits is called full adder.

HALF ADDER.

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$S = \bar{A}B + A\bar{B} = A \oplus B$

$C = AB$



* A combinational logic circuit which is used to add two binary bits is called Half adder.

* The two inputs are named A & B.
* The two outputs are named Sum & Carry. (S & C)
* If both the inputs are logic zero (low), then, output is logic zero for both outputs (Sum & Carry)
* If the both the inputs are different logic one or zero, then the Sum output is logic one (High), Carry output is zero (low).
* If both the inputs are logic one (High), then, the output sum is zero, and Carry logic one (high).

FULL ADDER.

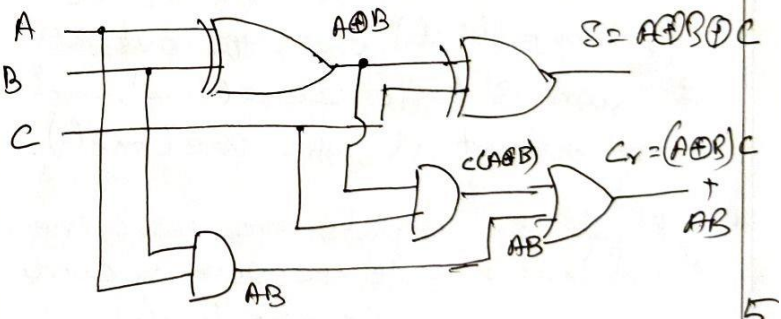
A	B	C	S	C_r
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$S = A \oplus B \oplus C$

$C_r = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

$C_r = AB + (A \oplus B)C$



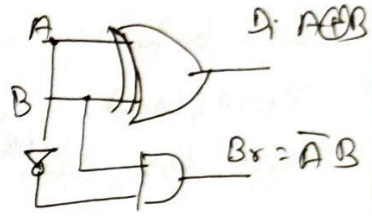
* Full adder means adding of three binary bits and outputs are sum and carry.
* If all the three inputs are logic zero (low), then, both the outputs of sum & carry are logic zero (low).
* If any one of the input is logic one (high) only one input. then, the output of sum is logic one (high) and carry output is logic zero (low).
* If any of the two inputs are logic one (high), then, the output of sum is logic zero (low), and carry output is logic one (high).
* If all the inputs are logic one (high), then, Both the sum & carry outputs are logic one (high).

SUBTRACTOR.

They are two types of subtractor circuits (i) Half subtractor, (ii) Full subtractor.

HALF-SUBTRACTOR.

A	B	B_r	D_i
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0



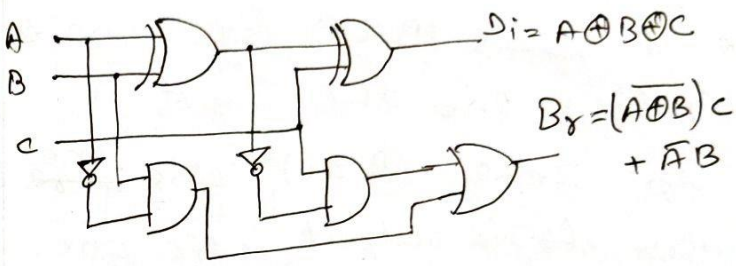
* If both the inputs are logic zero (low), then, output of both Borrow and Difference logic zero (low).
* If inputs A logic zero (low), and B Input B logic one (high), then outputs Difference and Borrow logic one (high).

* If input A, logic one(high) and input B, logic zero(low) then, output Borrow logic zero (low) and Difference logic one(high).

* If inputs are logic one(high) then. Outputs are both borrow & Difference logic zero.

~~FULL ADDE~~
FULL SUBTRACTOR.

A	B	C	Br	Di
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



* If all the inputs are ABC are logic zero(low), and inputs A&B, A&C are logic one(high), then outs are Borrow & Difference logic zero.

* If inputs (A&B), (A&C), ~~(A,B,C)~~ logic zero(low), the inputs A,B,C logic One(high) then, Outputs are both borrow & Difference logic one(high).

* If inputs (B & C) logic zero & A logic one and, input A logic zero, (B & C) logic one then, logic output logic one

* If inputs B & C are logic one and input A logic zero, then output Difference logic zero, & Borrow logic one.

* If inputs B & C logic zero by 'A' logic one then, output Borrow logic zero & Difference logic one.

SUM OF PRODUCT FORM.

1. $AB\bar{C} + A\bar{B}\bar{C}$
2. $XY + X\bar{Y}Z + YZ$
3. $\bar{P}Q + PQR + QRS$

PRODUCT OF SUM FORM.

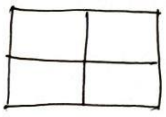
1. $(A+B+C)(A+\bar{B}+C)$
2. $(X+\bar{Y})(X+\bar{Y}+Z)(Y+\bar{Z})$
3. $(P+\bar{Q})(P+Q+R)(Q+\bar{R}+S)$

MINTERMS & MAXTERMS

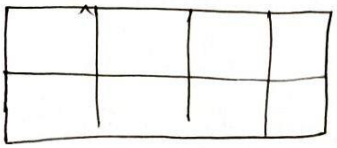
A	B	C	Minterms (m_i)	Maxterms (M_i)
0	0	0	$\bar{A}\bar{B}\bar{C} = m_0$	$A+B+C = M_0$
0	0	1	$\bar{A}\bar{B}C = m_1$	$A+B+\bar{C} = M_1$
0	1	0	$\bar{A}B\bar{C} = m_2$	$A+\bar{B}+C = M_2$

A	B	C	Minterms (m_i)	Maxterms (M_i)
0	1	1	$\bar{A}BC = m_3$	$A+\bar{B}+\bar{C} = M_3$
1	0	0	$A\bar{B}\bar{C} = m_4$	$\bar{A}+B+C = M_4$
1	0	1	$A\bar{B}C = m_5$	$\bar{A}+B+\bar{C} = M_5$
1	1	0	$AB\bar{C} = m_6$	$\bar{A}+\bar{B}+C = M_6$
1	1	1	$ABC = m_7$	$\bar{A}+\bar{B}+\bar{C} = M_7$

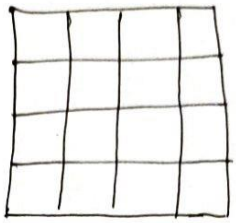
KARNAUGH MAP (K-MAP)



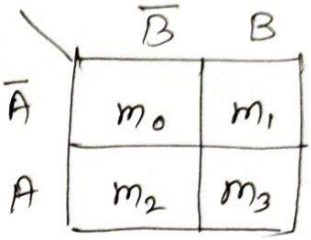
2-Variable Map (4-cells)



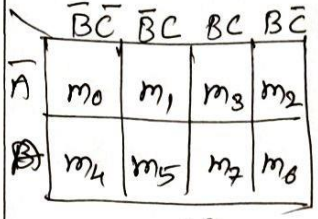
3-Variable Map (8-cells)



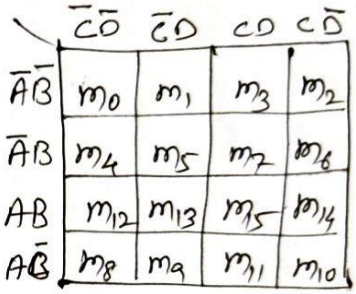
4-Variable Map (16-cells)



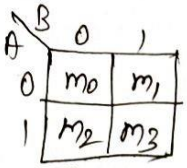
2-Variable Map.

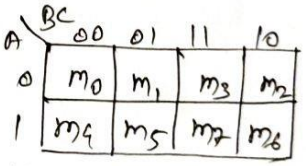


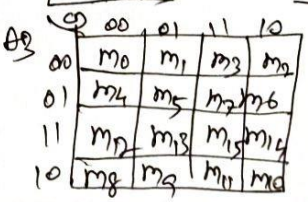
3-Variable Map



4-Variable Map.







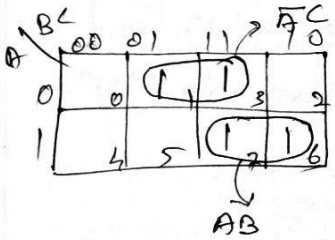
GROPING CELLS FOR SIMPLIFICATION.

PAIR - Grouping two adjacent ones.

QUAD! Grouping four adjacent ones.

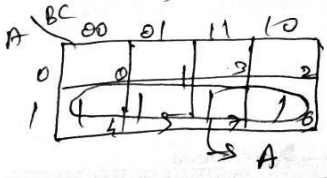
OCTET: Grouping eight adjacent ones.

1. $f(A,B,C) = \Sigma m(1,3,6,7)$



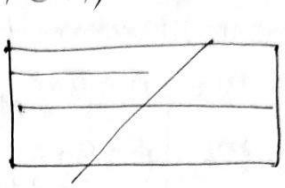
$f = \bar{A}C + AB.$

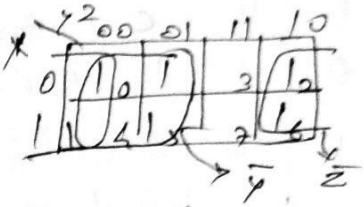
2. $f(A,B,C) = \Sigma m(4,5,6,7)$



$f = A$

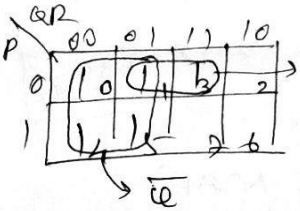
3. $f(X,Y,Z) = \Sigma m(0,1,2,4,5,6)$





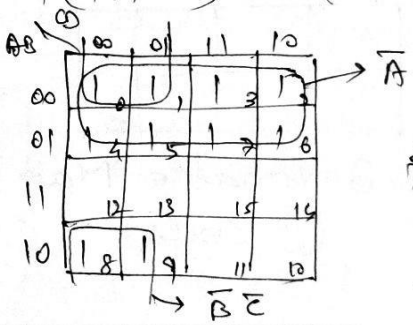
$f = \bar{Y} + \bar{Z}$

4. $f(P,Q,R) = \Sigma m(0,1,3,4,5)$



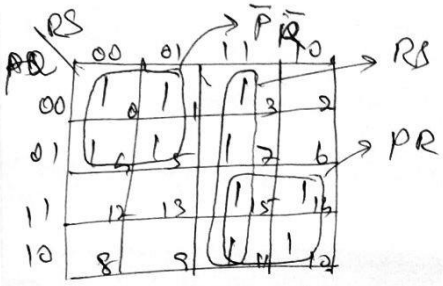
$f = \bar{Q} + \bar{P}R$

1. $f(A,B,C,D) = \Sigma m(0,1,2,3,4,5,6,7,8,9)$



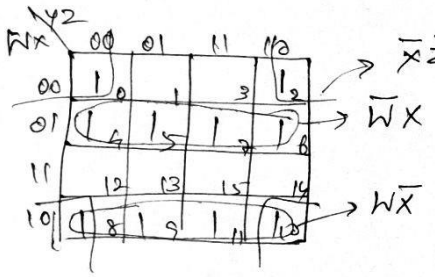
$f = \bar{A} + \bar{B}\bar{C}$

2. $f(P,Q,R,S) = \Sigma m(0,1,3,4,5,7,10,11,14,15)$



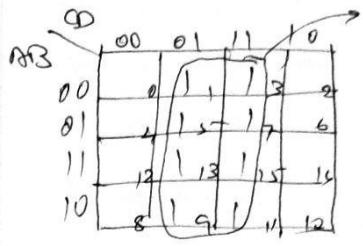
$f = \bar{P}\bar{R} + RS + PR$

3. $f(W,X,Y,Z) = \Sigma m(0,2,4,5,6,7,8,9,10,11)$



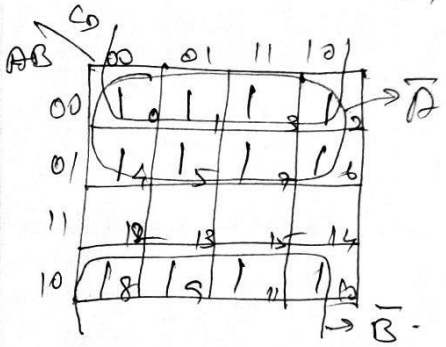
$f = \bar{W}X + W\bar{X} + \bar{X}\bar{Z}$

4. $f(A,B,C,D) = \Sigma m(1,3,5,7,13,15,9,11)$



$f = D$

5. $f(A,B,C,D) = \Sigma m(0,1,2,4,5,6,8,9,10,3,7,11)$



$f = \bar{A} + \bar{B}$